Features

- First USB Host/Slave controller for embedded systems in the market with a standard microprocessor bus interface
- Supports both full speed (12 Mbps) and low speed (1.5 Mbps) USB transfer in both master and slave modes
- Conforms to USB Specification 1.1 for full- and low speed
- Operates as a single USB host or slave under software control
- Automatic detection of either low- or full-speed devices
- 8-bit bidirectional data, port I/O (DMA supported in slave mode)
- On-chip SIE and USB transceivers
- On-chip single root HUB support
- 256-byte internal SRAM buffer
- Ping-pong buffers for improved performance
- Operates from 12 or 48 MHz crystal or oscillator (built-in DPLL)
- 5 V-tolerant interface
- Suspend/resume, wake up, and low-power modes are supported
- Auto-generation of SOF and CRC5/16
- Auto-address increment mode, saves memory READ/ WRITE cycles
- Development kit including source code drivers is available
- 3.3-V power source, 0.35 micron CMOS technology
- Available in 48-pin TQFP package

Functional Description

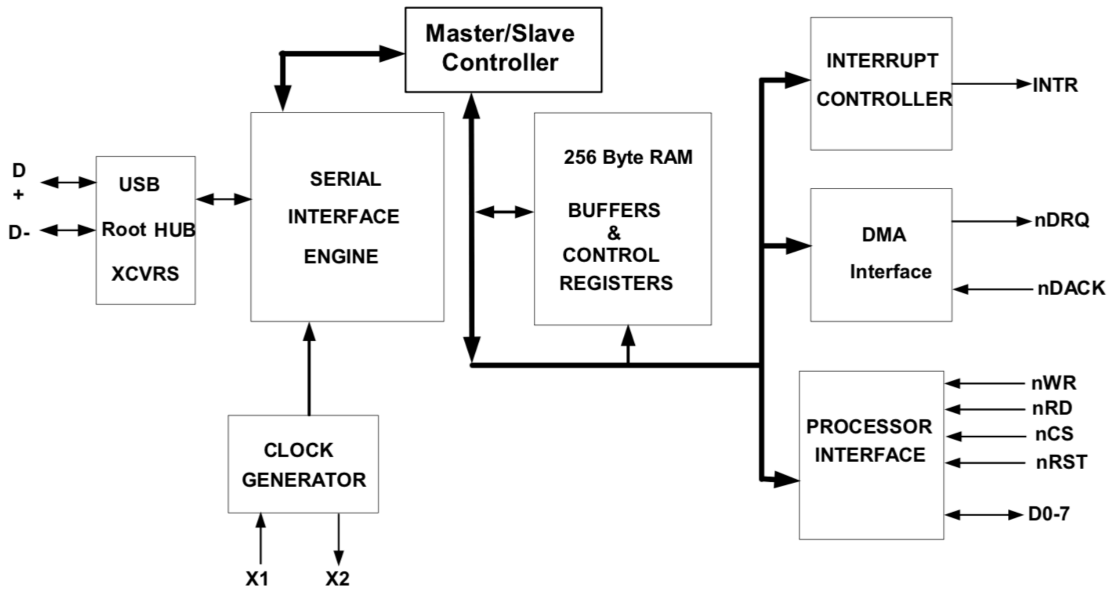
The CLM811HST-AXC is an Embedded USB Host/Slave Controller capable of communicating in either full speed or low speed. The CLM811HST-AXC interfaces to devices such as microprocessors, micro- controllers, DSPs, or directly to a variety of buses such as ISA, PCMCIA, and others. The CLM811HST-AXC USB Host Controller conforms to USB Specification 1.1.

The CLM811HST-AXC incorporates USB Serial Interface functionality along with internal full or low speed transceivers. The CLM811HST-AXC supports and operates in USB full speed mode at 12 Mbps, or in low-speed mode at 1.5 Mbps. When in host mode, the CLM811HST-AXC is the master and controls the USB bus and the devices that are connected to it. In peripheral mode, otherwise known as a slave device, the CLM811HST-AXC operates as a variety of full- or low-speed devices.

The CLM811HST-AXC data port and microprocessor interface provide an 8-bit data path I/O or DMA bidirectional, with interrupt support to allow easy interface to standard microprocessors or microcontrollers such as Motorola or Intel CPUs and many others. The CLM811HST-AXC has 256 bytes of internal RAM, which is used for control registers and data buffers.

The available Pb-free package is a 48-pin (CLM811HST-AXC) package. All packages operate at 3.3 VDC. The I/O interface logic is 5 V-tolerant.

Logic Block Diagram



Functional Overview

Data Port, Microprocessor Interface

The CLM811HST-AXC[1] microprocessor interface provides an 8-bit bidirectional data path along with appropriate control lines to interface to external processors or controllers. Programmed I/O or memory mapped I/O designs are supported through the 8-bit interface, chip select, read and write input strobes, and a single address line, A0.

Access to memory and control register space is a simple two step process, requiring an address Write with A0 = ‘0’, followed by a register/memory Read or Write cycle with address line A0 = ‘1’.

In addition, a DMA bidirectional interface in slave mode[2] is available with handshake signals such as nDRQ, nDACK, nWR, nRD, nCS and INTRQ.

The CLM811HST-AXC WRITE or READ operation terminates when either nWR or nCS goes inactive. For devices interfacing to the CLM811HST-AXC that deactivate the Chip Select nCS before the Write nWR, the data hold timing must be measured from the nCS and is the same value as specified. Therefore, both Intel®-and Motorola-type CPUs work easily with the CLM811HST-AXC without any external glue logic requirements.

DMA Controller (slave mode only)

In applications that require transfers of large amount of data, such as scanner interfaces, the CLM811HST-AXC provides a DMA interface. This interface supports DMA READ or WRITE transfers to the CLM811HST-AXC internal RAM buffer, it is done through the microprocessor data bus via two control lines (nDRQ - Data Request and nDACK - Data Acknowledge), along with the nWR line and controls the data flow into the CLM811HST-AXC. The CLM811HST-AXC has a count register that allows selection of programmable block sizes for DMA transfer. The control signals, both nDRQ and nDACK, are designed for compatibility with standard DMA interfaces.

Interrupt Controller

The CLM811HST-AXC interrupt controller provides a single output signal (INTRQ) that is activated by a number of programmable events that may occur as a result of USB activity. Control and status registers are provided to allow the user to select single or multiple events, which generate an interrupt (assert INTRQ) and let the user view interrupt status. The interrupts are cleared by writing to the Interrupt Status Register.

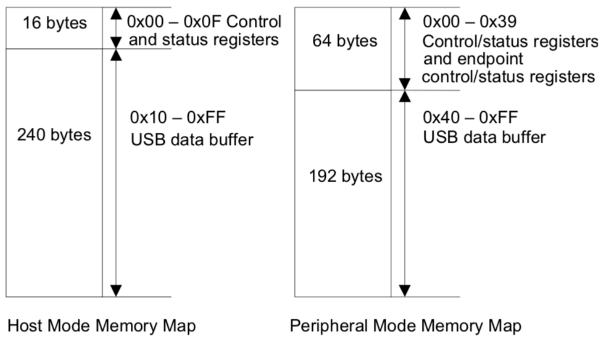
Buffer Memory

The CLM811HST-AXC contains 256 bytes of internal memory used for USB data buffers, control registers, and status registers. When in master mode (host mode), the memory is defined where the first 16 bytes are registers and the remaining 240 bytes are used for USB data buffers. When in slave mode (peripheral mode), the first 64 bytes are used for the four endpoint control and status registers along with the various other registers. This leaves 192 bytes of endpoint buffer space for USB data transfers.

Access to the registers and data memory is through the 8-bit external microprocessor data bus, in either indexed or direct addressing. Indexed mode uses the Auto Address Increment mode described in Auto Address Increment Mode [3], where direct addressing is used to READ/WRITE to an individual address.

USB transactions are automatically routed to the memory buffer that is configured for that transfer. Control registers are provided so that pointers and block sizes in buffer memory are determined and allocated.

Figure 1. Memory Map



Auto Address Increment Mode [3]

The CLM811HST-AXC supports the auto increment mode to reduce READ and WRITE memory cycles. In this mode, the microcontroller needs to set up the address only once. Whenever any subsequent DATA is accessed, the internal address counter advances to the next address location.

Auto Address Increment Example. To fill the data buffer that is configured for address 10h, follow these steps:

1. Write 10h to CLM811HST-AXC with A0 LOW. This sets the memory address that is used for the next operation.
2. Write the first data byte into address 10h by doing a write operation with A0 HIGH. An example is a Get Descriptor; the first byte that is sent to the device is 80h (bmRequestType) so you would write 80h to address 10h.
3. Now the internal RAM address pointer is set to 11h. So, by doing another write with A0 HIGH, RAM address location 11h is written with the data. Continuing with the Get Descriptor example, a 06h is written to address 11h for the bRequest value.
4. Repeat Step 3 until all the required bytes are written as necessary for a transfer. If auto-increment is not used, you write the address value each time before writing the data as shown in Step 1.

The advantage of the auto address increment mode is that it reduces the number of required CLM811HST-AXC memory READ/WRITE cycles to move data to/from the device. For example, transferring 64 bytes of data to/from CLM811HST-AXC, using auto increment mode, reduces the number of cycles to 1 address WRITE and 64 READ/WRITE data cycles, compared to 64 address writes and 64 data cycles for random access.

PLL Clock Generator

Either a 12-MHz [4] or a 48-MHz external crystal is used with the CLM811HST-AXC [5]. Two pins, X1 and X2, are provided to connect a low cost crystal circuit to the device as shown in Figure 2 and Figure 3. Use an external clock source if available in the application instead of the crystal circuit by connecting the source directly to the X1 input pin. When a clock is used, the X2 pin is not connected.

When the CM pin is tied to a logic 0, the internal PLL is bypassed so the clock source must meet the timing requirements specified by the USB specification.

Figure 2. Full Speed 48 MHz Crystal Circuit

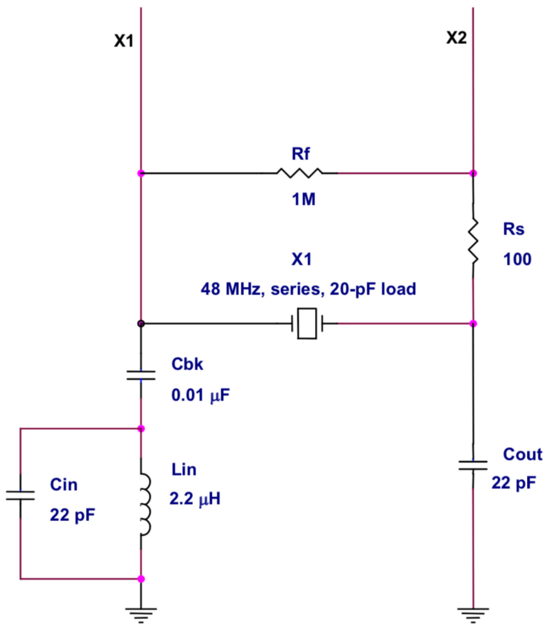
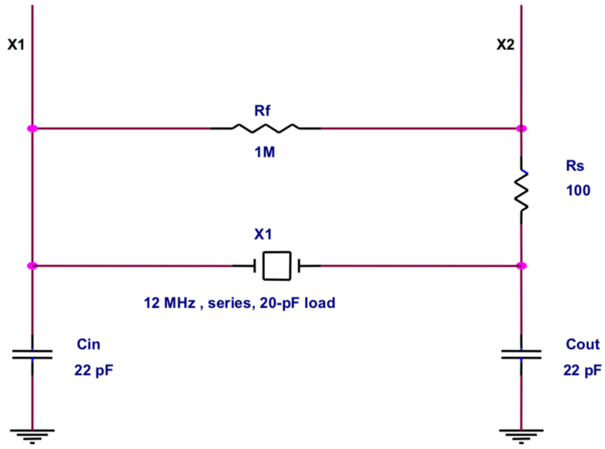


Figure 3. Optional 12 MHz Crystal Circuit



Typical Crystal Requirements

The following are examples of 'typical requirements.' Note that these specifications are generally found as standard crystal values and are less expensive than custom values. If crystals are used in series circuits, load capacitance is not applicable. Load capacitance of parallel circuits is a requirement. The 48-MHz third overtone crystals require the Cin/Lin filter to guarantee 48-MHz operation.

12 MHz Crystals:

Frequency Tolerance:	±100 ppm or
better Operating Temperature Range:	0 °C to 70 °C
Frequency:	12 MHz
Frequency Drift over Temperature:	± 50 ppm ESR
(Series Resistance):	60 Ω
Load Capacitance:	10 pF min
Shunt Capacitance:	7 pF max
Drive Level:	0.1–0.5 mW
Operating Mode:	fundamental

48 MHz Crystals:

Frequency Tolerance:	±100 ppm or
better Operating Temperature Range:	0 °C to 70 °C
Frequency:	48 MHz
Frequency Drift over Temperature:	± 50 ppm ESR
(Series Resistance):	40 Ω
Load Capacitance:	10 pF min
Shunt Capacitance:	7 pF max
Drive Level:	0.1–0.5 mW
Operating Mode:	third overtone

USB Transceiver

The CLM811HST-AXC has a built-in transceiver that meets USB Specification 1.1. The transceiver is capable of transmitting and receiving serial data at USB full speed [6] (12 Mbits) and low speed [7] (1.5 Mbits). The driver portion of the transceiver is differential while the receiver section is comprised of a differential receiver and two single-ended receivers. Internally, the transceiver interfaces to the Serial Interface Engine (SIE) logic. Externally, the transceiver connects to the physical layer of the USB.

CLM811HST-AXC Registers

Operation and control of the CLM811HST-AXC is managed through internal registers. When operating in Master/Host mode, the first 16 address locations are defined as register space. In Slave/Peripheral mode, the first 64 bytes are defined as register space. The register definitions vary greatly between each mode of operation and are defined separately in this document (section Table 1 describes Host register definitions, while Table 19 on page 15 describes Slave register definitions). Access to the registers are through the microprocessor interface similar to normal RAM accesses (see "Bus Interface Timing Requirements" on page 26) and provide control and status information for USB transactions.

Any write to control register 0FH enables the CLM811HST-AXC full features bit. This is an internal bit of the CLM811HST-AXC that enables additional features.

Table 1 shows the memory map and register mapping of the CLM811HST-AXC in master/host mode.

Table 1. CLM811HST-AXC Master (Host) Mode Registers

Register Name CLM811HST-AXC	CLM811HST-AXC (hex) Address
USB-A Host Control Register	00h
USB-A Host Base Address	01h
USB-A Host Base Length	02h
USB-A Host PID, Device Endpoint (Write)/USB Status (Read)	03h
USB-A Host Device Address (Write)/ Transfer Count (Read)	04h
Control Register 1	05h
Interrupt Enable Register	06h
Reserved Register	Reserved
USB-B Host Control Register	08h
USB-B Host Base Address	09h
USB-B Host Base Length	0Ah
USB-B Host PID, Device Endpoint (Write)/USB Status (Read)	0Bh
USB-B Host Device Address (Write)/ Transfer Count (Read)	0Ch
Status Register	0Dh
SOF Counter LOW (Write)/HW Revision Register (Read)	0Eh
SOF Counter HIGH and Control Register 2	0Fh
Memory Buffer	10H-FFh

The registers in the CLM811HST-AXC are divided into two major groups. The first group is referred to as USB Control registers. These registers enable and provide status for control of USB transactions and data flow. The second group of registers provides control and status for all other operations.

Register Values on Power-up and Reset

The following registers initialize to zero on power-up and reset:

- USB-A/USB-B Host Control Register [00H, 08H] bit 0 only
- Control Register 1 [05H]
- USB Address Register [07H]
- Current Data Set/Hardware Revision/SOF Counter LOW Register [0EH]

All other register's power-up and reset in an unknown state and firmware for initialization.

USB Control Registers

Communication and data flow on the USB bus uses the CLM811HST-AXC' USB A-B Control registers. The CLM811HST-AXC communi- cates with any USB Device function and any specific endpoint via the USB-A or USB-B register sets.

The USB A-B Host Control registers are used in an overlapped configuration to manage traffic on the USB bus. The USB Host Control register also provides a means to interrupt an external CPU or microcontroller when one of the USB protocol transac- tions is completed. Table 1 and Table 2 show the two sets of USB Host Control registers, the 'A' set and 'B' set. The two register sets allow for overlapping operation. When one set of param- eters is being set up, the other is transferring. On completion of a transfer to an endpoint, the next operation is controlled by the other register set.

Note The USB-B register set is used only when CLM811HST-AXC mode is enabled by initializing register 0FH.

The CLM811HST-AXC USB Host Control has two groups of five registers each which map in the CLM811HST-AXC memory space. These registers are defined in the following tables.

Register Name CLM811H	CLM811HST-AXC (hex) Address
USB-A Host Control Register	00h
USB-A Host Base Address	01h
USB-A Host Base Length	02h
USB-A Host PID, Device Endpoint (Write)/USB Status (Read)	03h
USB-A Host Device Address (Write)/ Transfer Count (Read)	04h
USB-B Host Control Register	08h
USB-B Host Base Address	09h
USB-B Host Base Length	0Ah
USB-B Host PID, Device Endpoint (Write)/USB Status (Read)	0Bh
USB-B Host Device Address (Write)/ Transfer Count (Read)	0Ch

Table 2. CLM811HST-AXC Host Control Registers

USB-A/USB-B Host Control Registers [Address = 00h, 08h] .

Table 3. USB-A/USB-B Host Control Register Definition [Address 00h, 08h]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Preamble	Data Toggle Bit	SyncSOF	ISO	Reserved	Direction	Enable	Arm

Bit Position	Bit Name	Functi on
7	Preamble	If bit = '1' a preamble token is transmitted before transfer of low speed packet. If bit = '0', preamble generation is disabled. ▪ The CLM811HST-AXC automatically generates preamble packets when bit 7 is set. This bit is only used to send packets to a low speed device through a hub. To communicate to a full speed device, this bit is set to '0'. For example, when CLM811HST-AXC communicates to a low speed device via the HUB: — Set CLM811HST-AXC SIE to operate at full speed, i.e., bit 5 of register 05h (Control Register 1) = '0'. — Set bit 6 of register 0Fh (Control Register 2) = '0'. Set correct polarity of DATA+ and DATA– state for full speed. — Set bit 7, Preamble bit, = '1' in the Host Control register. ▪ When CLM811HST-AXC communicates directly to a low speed device: — Set bit 5 of register 05h (Control Register 1) = '1'. — Set bit 6 of register 0Fh (Control Register 2) = '1', DATA+ and DATA– polarity for low speed. — The state of bit 7 is ignored in this mode.
6	Data Toggle Bit	'0' if DATA0, '1' if DATA1 (only used for OUT tokens in host mode).
5	SyncSOF	'1' = Synchronize with the SOF transfer when operating in FS only. The CLM811HST-AXC uses bit 5 to enable transfer of a data packet after a SOF packet is transmitted. When bit 5 = '1', the next enabled packet is sent after next SOF. If bit 5 = '0' the next packet is sent immediately if the SIE is free. If operating in low speed, do not set this bit.
4	ISO	When set to '1', this bit allows Isochronous mode for this packet.
3	Reserved	Bit 3 is reserved for future use.
2	Direction	When equal to '1' transmit (OUT). When equal to '0' receive (IN).
1	Enable	If Enable = '1', this bit allows transfers to occur. If Enable = '0', USB transactions are ignored. The Enable bit is used in conjunction with the Arm bit (bit 0 of this register) for USB transfers.
0	Arm	Allows enabled transfers when Arm = '1'. Cleared to '0' when transfer is complete (when Done Interrupt is asserted).

Once the other CLM811HST-AXC Control registers are configured (registers 01h-04h or 09h-0Ch) the Host Control register is programmed to initiate the USB transfer. This register initiates the transfer when the Enable and Arm bit are set as described above.

USB-A/USB-B Host Base Address [Address = 01h, 09h] .

Table 4. USB-A/USB-B Host Base Address Definition [Address 01h, 09h]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HBADD7	HBADD6	HBADD5	HBADD4	HBADD3	HBADD2	HBADD1	HBADD0

The USB-A/B Base Address is a pointer to the CLM811HST-AXC memory buffer location for USB reads and writes. When transferring data OUT (Host to Device), the USB-A and USB-B Host Base Address registers can be set up before setting ARM on the USB-A or USB-B Host Control register. When using a double buffer scheme, the Host Base Address could be set up with the first buffer used for DATA0 data and the other for DATA1 data.

USB-A/USB-B Host Base Length [Address = 02h, 0Ah].
Table 5. USB-A / USB-B Host Base Length Definition [Address 02h, 0Ah]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HBL7	HBL6	HBL5	HBL4	HBL3	HBL2	HBL1	HBL0

The USB A/B Host Base Length register contains the maximum packet size transferred between the CLM811HST-AXC and a slave USB peripheral. Essentially, this designates the largest packet size that is transferred by the CLM811HST-AXC. Base Length designates the size of data packet sent or received. For example, in full speed BULK mode, the maximum packet length is 64 bytes. In ISO mode, the maximum packet length is 1023 bytes since the CLM811HST-AXC only has an 8-bit length; the maximum packet size for the ISO mode using the CLM811HST-AXC is 255 – 16 bytes (register space). When the Host Base length register is set to zero, a Zero-Length packet is transmitted.

USB-A/USB-B USB Packet Status (Read) and Host PID, Device Endpoint (Write) [Address = 03h, 0Bh]. This register has two modes dependent on whether it is read or written. When read, this register provides packet status and contains information relative to the last packet that has been received or transmitted. This register is not valid for reading until after the Done interrupt occurs, which causes the register to update.

Table 6. USB-A/USB-B USB Packet Status Register Definition when READ [Address 03h, 0Bh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STALL	NAK	Overflow	Setup	Sequence	Time-out	Error	ACK

Bit Position	Bit Name	Functi on
7	STALL	Slave device returned a STALL.
6	NAK	Slave device returned a NAK.
5	Overflow	Overflow condition - maximum length exceeded during receives. For underflow, see USB-A/USB-B Host Transfer Count Register (Read), USB Address (Write) [Address = 04h, 0Ch].
4	Setup	This bit is not applicable for Host operation since a SETUP packet is generated by the host.
3	Sequence	Sequence bit. '0' if DATA0, '1' if DATA1.
2	Time-out	Timeout occurred. A timeout is defined as 18-bit times without a device response (in full speed).
1	Error	Error detected in transmission. This includes CRC5, CRC16, and PID errors.
0	ACK	Transmission Acknowledge.

When written, this register provides the PID and Endpoint information to the USB SIE engine used in the next transaction. All 16 Endpoints can be addressed by the CLM811HST-AXC.
Table 7. USB-A / USB-B Host PID and Device Endpoint Register when WRITTEN [Address 03h, 0Bh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PID3	PID2	PID1	PID0	EP3	EP2	EP1	EP0

PID[3:0]: 4-bit PID Field (See following table), EP[3:0]: 4-bit Endpoint Value in Binary.

PID TYPE	D7–D4
SETUP	1101 (D Hex)
IN	1001 (9 Hex)
OUT	0001 (1 Hex)
SOF	0101 (5 Hex)
PREAMBLE	1100 (C Hex)
NAK	1010 (A Hex)
STALL	1110 (E Hex)
DATA0	0011 (3 Hex)
DATA1	1011 (B Hex)

USB-A/USB-B Host Transfer Count Register (Read), USB Address (Write) [Address = 04h, 0Ch]. This register has two different functions depending on whether it is read or written. When read, this register contains the number of bytes remaining (from Host Base Length value) after a packet is transferred. For example, if the Base Length register is set to 0x040 and an IN Token was sent to the peripheral device. If, after the transfer is complete, the value of the Host Transfer Count is 0x10, the number of bytes actually transferred is 0x30. This is considered as an underflow indication.

Table 8. USB-A / USB-B Host Transfer Count Register when READ [Address 04h, 0Ch]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HTC7	HTC6	HTC5	HTC4	HTC3	HTC2	HTC1	HTC0

When written, this register contains the USB Device Address with which the Host communicates.

Table 9. USB-A / USB-B USB Address when WRITTEN [Address 04h, 0Ch]

Bit 7	Bit 6	Bit 5	Bit 4	Bit3	Bit 2	Bit 1	Bit 0
0	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA6-DA0 Device address, up to 127 devices can be

addressed. DA7 Reserved bit must be set to zero.

CLM811HST-AXC Control Registers

The next set of registers are the Control registers and control more of the operation of the chip instead of USB packet type of transfers. Table 10 is a summary of the control registers.

Table 10. Control Registers Summary

Register Name CLM811H	CLM811HST-AXC (hex) Address
Control Register 1	05h
Interrupt Enable Register	06h
Reserved Register	07h
Status Register	0Dh
SOF Counter LOW (Write)/HW Revision Register (Read)	0Eh
SOF Counter HIGH and Control Register 2	0Fh
Memory Buffer	10h-FFh

Control Register 1 [Address = 05h]. The Control Register 1 enables/disables USB transfer operation with control bits defined as follows.

Table 11. Control Register 1 [Address 05h]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Suspend	USB Speed	J-K state force	USB Engine Reset	Reserved	Reserved	SOF ena/dis

Bit Position	Bit Name	Function
7	Reserved	‘0’
6	Suspend	’1’ = enable, ‘0’ = disable.
5	USB Speed	’0’ setup for full speed, ‘1’ setup low speed.
4	J-K state force	See Table 12.
3	USB Engine Reset	USB Engine reset = ‘1’. Normal set ‘0’. When a device is detected, the first thing that to do is to send it a USB Reset to force it into its default address of zero. The USB 2.0 specification states that for a root hub a device must be reset for a minimum of 50 mS.
2	Reserved	Some existing firmware examples set bit 2, but it is not necessary.
1	Reserved	‘0’
0	SOF ena/dis	’1’ = enable auto Hardware SOF generation; ‘0’ = disable. In the CLM811HST-AXC, bit 0 is used to enable hardware SOF auto-generation. The generation of SOFs continues when set to ‘0’, but SOF tokens are not output to USB.

At power-up this register is cleared to all zeros.

Low-power Modes [Bit 6 Control Register, Address 05h]

When bit 6 (Suspend) is set to ‘1’, the power of the transmit transceiver is turned off, the internal RAM is in suspend mode, and the internal clocks are disabled.

Note Any activity on the USB bus (that is, K-State, etc.) resumes normal operation. To resume normal operation from the CPU side, a Data Write cycle (i.e., A0 set HIGH for a Data Write cycle) is done. This is a special case and not a normal direct write where the address is first written and then the data. To resume normal operation from the CPU side, you must do a Data Write cycle only.

Low Speed/Full Speed Modes [Bit 5 Control Register 1, Address 05h]

The CLM811HST-AXC is designed to communicate with either full- or low speed devices. At power-up bit 5 is LOW, i.e., for full speed.

There are two cases when communicating with a low speed device. When a low speed device is connected directly to the CLM811HST-AXC, bit 5 of Register 05h is set to ‘1’ and bit 6 of register 0Fh, Polarity Swap, is set to ‘1’ in order to change the polarity of D+ and D–. When a low speed device is connected via a HUB to CLM811HST-AXC, bit 5 of Register 05h is set to ‘0’ and bit 6 of register 0Fh is set to ’0’ in order to keep the polarity of D+ and D– for full speed. In addition, make sure that bit 7 of USB-A/USB-B Host Control registers [00h, 08h] is set to ‘1’ for preamble generation.

J-K Programming States [Bits 4 and 3 of Control Register 1, Address 05h]

The J-K force state control and USB Engine Reset bits are used to generate a USB reset condition. Forcing K-state is used for Peripheral device remote wake up, resume, and other modes. These two bits are set to zero on power-up.

Table 12. Bus Force States

USB Engine Reset	J-K Force State	Function
0	0	Normal operating mode
0	1	Force USB Reset, D+ and D– are set LOW (SE0)
1	0	Force J-State, D+ set HIGH, D– set LOW[8]
1	1	Force K-State, D– set HIGH, D+ set LOW[9]

Notes
8. Force K-State for low speed.
9. Force J-State for low speed.

USB Reset Sequence

After a device is detected, write 08h to the Control register (05h) to initiate the USB reset, then wait for the USB reset time (root hub should be 50 ms) and additionally some types of devices such as a Forced J-state. Lastly, set the Control register (05h) back to 0h. After the reset is complete, the auto-SOF generation is enabled.

SOF Packet Generation

The CLM811HST-AXC automatically computes the frame number and CRC5 by hardware. No CRC or SOF generation is required by external firmware for the CLM811HST-AXC, although it can be done by sending an SOF PID in the Host PID, Device Endpoint register.

To enable SOF generation, assuming host mode is configured:

1. Set up the SOF interval in registers 0x0F and 0x0E.
2. Enable the SOF hardware generation in this register by setting bit 0 = ‘1’.
3. Set the Arm bit in the USB-A Host Control register.

Interrupt Enable Register [Address = 06h]. The CLM811HST-AXC provides an Interrupt Request Output, which is activated for a number of conditions. The Interrupt Enable register allows the user to select conditions that result in an interrupt that is issued to an external CPU through the INTRQ pin. A separate Interrupt Status register reflects the reason for the interrupt. Enabling or disabling these interrupts does not have an effect on whether or not the corresponding bit in the Interrupt Status register is set or cleared; it only determines if the interrupt is routed to the INTRQ pin. The Interrupt Status register is normally used in conjunction with the Interrupt Enable register and can be polled in order to determine the conditions that initiated the interrupt (See the description for the Interrupt Status Register). When a bit is set to ’1’ the corresponding interrupt is enabled. So when the enabled interrupt occurs, the INTRQ pin is asserted. The INTRQ pin is a level interrupt, meaning it is not deasserted until all enabled interrupts are cleared.

Table 13. Interrupt Enable Register [Address 06h]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Device Detect/ Resum e	Inserte d/ Remov ed	SOF Timer	Reserved	Reserved	USB -B DO NE	USB -A DO NE

Bit Position	Bit Name	Function
7	Reserved	‘0’
6	Device Detect/ Resume	Enable Device Detect/Resume Interrupt. When bit 6 of register 05h (Control Register 1) is equal to ’1’, bit 6 of this register enables the Resume Detect Interrupt. Otherwise, this bit is used to enable Device Detection status as defined in the Interrupt Status register bit definitions.
5	Inserted/Removed	Enable Slave Insert/Remove Detection is used to enable/disable the device inserted/removed interrupt.
4	SOF Timer	1 = Enable Interrupt for SOF Timer. This is typically at 1 mS intervals, although the timing is determined by the SOF Counter high/low registers. To use this bit function, bit 0 of register 05h must be enabled and the SOF counter registers 0E hand 0Fh must be initialized.
3	Reserved	‘0’
2	Reserved	‘0’
1	USB-B DONE	USB-B Done Interrupt (see USB-A Done interrupt).
0	USB-A DONE	USB-A Done Interrupt. The Done interrupt is triggered by one of the events that are logged in the USB Packet Status register. The Done interrupt causes the Packet Status register to update.

USB Address Register, Reserved, Address [Address = 07h]. This register is reserved for the device USB Address in Slave operation. It should not be written by the user in host mode.

Registers 08h-0Ch Host-B registers. Registers 08h-0Ch have the same definition as registers 00h-04h except they apply to Host-B instead of Host-A.

Interrupt Status Register, Address [Address = 0Dh]. The Interrupt Status register is a READ/WRITE register providing interrupt status. Interrupts are cleared by writing to this register. To clear a specific interrupt, the register is written with corresponding bit set to '1'.

Table 14. Interrupt Status Register [Address 0Dh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D+	Device Detect/ Resum e	Insert/ Remove	SOF timer	Reserved	Reserved	USB-B	USB-A

Bit Position	Bit Name	Functi on
7	D+	Value of the Data+ pin. Bit 7 provides continuous USB Data+ line status. Once it is determined that a device is inserted (as described below) with bits 5 and 6, bit 7 is used to detect if the inserted device is low speed (0) or full speed (1).
6	Device Detect/ Resume	Device Detect/Resume Interrupt. Bit 6 is shared between Device Detection status and Resume Detection interrupt. When bit-6 of register 05h is set to one, this bit is the Resume detection Interrupt bit. Otherwise, this bit is used to indicate the presence of a device, '1' = device 'Not present' and '0' = device 'Present.' In this mode, check this bit along with bit 5 to determine whether a device has been inserted or removed.
5	Insert/Remove	Device Insert/Remove Detection. Bit 5 is provided to support USB cable insertion/removal for the CLM811HST-AXC in host mode. This bit is set when a transition from SE0 to IDLE (device inserted) or from IDLE to SE0 (device removed) occurs on the bus.
4	SOF timer	'1' = Interrupt on SOF Timer.
3	Reserved	'0'
2	Reserved	'0'
1	USB-B	USB-B Done Interrupt. (See description in Interrupt Enable Register [address 06h].)
0	USB-A	USB-A Done Interrupt. (See description in Interrupt Enable Register [address 06h].)

Current Data Set Register/Hardware Revision/SOF Counter LOW [Address = 0Eh]. This register has two modes. Read from this register indicates the current CLM811HST-AXC silicon revision.

Table 15. Hardware Revision when Read [Address 0Eh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Hardware Revision				Reserved			

Bit Position	Bit Name	Function
7-4	Hardware Revision	CLM811HST-AXC rev1.2 Read = 1H; CLM811HST-AXC rev1.5 Read = 2.
3-2	Reserved	Read is zero.
1-0	Reserved	Reserved for slave.

Writing to this register sets up auto generation of SOF to all connected peripherals. This counter is based on the 12 MHz clock and is not dependent on the crystal frequency. To set up a 1 ms timer interval, the software must set up both SOF counter registers to the proper values.

Table 16. SOF Counter LOW Address when Written [Address 0Eh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SOF7	SOF6	SOF5	SOF4	SOF3	SOF2	SOF1	SOF0

Example: To set up SOF for 1 ms interval, SOF counter register 0Eh should be set to E0h.

SOF Counter High/Control Register 2 [Address = 0Fh]. When read, this register returns the value of the SOF counter divided by
64. The software must use this register to determine the available bandwidth in the current frame before initiating any USB transfer. In this way, the user is able to avoid babble conditions on the USB. For example, to determine the available bandwidth left in a frame do the following.

Maximum number of clock ticks in 1 ms time frame is 12000 (1 count per 12 MHz clock period, or approximately 84 ns.) The value read back in Register 0FH is the (count × 64) × 84 ns = time remaining in current frame. USB bit time = one 12 MHz period.

Value of register 0FH	Available bit times left are between
BBH	12000 bits to 11968 (187 × 64) bits
BAH	11968 bits to 11904 (186 × 64) bits

Note: Any write to the 0Fh register clears the internal frame counter. Write register 0Fh at least once after power-up. The internal frame counter is incremented after every SOF timer tick. The internal frame counter is an 11-bit counter, which is used to track the frame number. The frame number is incremented after each timer tick. Its contents are transmitted to the slave every millisecond in a SOF packet.

Table 17. SOF High Counter when Read [Address 0Fh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C13	C12	C11	C10	C9	C8	C7	C6

When writing to this register the bits definition are defined as follows.

Table 18. Control Register 2 when Written [Address 0Fh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLM811HST-AXC Master/ Slave selection	CLM811HST-AXC D+/D– Data Polarity Swap	SOF High Counter Register					

Bit Position	Bit Name	Function
7	CLM811HST-AXC Master/Slave selection	Master = 1, Slave = 0.
6	CLM811HST-AXC D+/D– Data Polarity Swap	'1' = change polarity (low speed) '0' = no change of polarity (full speed).
5-0	SOF High Counter Register	Write a value or read it back to SOF High Counter Register.

Note Any write to Control register 0Fh enables the CLM811HST-AXC full features bit. This is an internal bit of the CLM811HST-AXC that enables additional features.

The USB-B register set is used when CLM811HST-AXC full feature bit is enabled.

Example. To set up host to generate 1 ms SOF time:

The register 0Fh contains the upper 6 bits of the SOF timer. Register 0Eh contains the lower 8 bits of the SOF timer. The timer is based on an internal 12-MHz clock and uses a counter, which counts down to zero from an initial value. To set the timer for 1 ms time, the register 0Eh is loaded with value E0h and register 0Fh (bits 0–5) is loaded with 2Eh. To start the timer, bit 0 of register 05h (Control Register 1) is set to '1', which enables hardware SOF generation. To load both HIGH and LOW registers with the proper values, the user must follow this sequence:

1. Write E0h to register 0Eh. This sets the lower byte of the SOF counter
2. Write AEh to register 0Fh, AEh configures the part for full speed (no change of polarity) Host with bits 5–0 = 2Ehfor upper portion of SOF counter.
3. Enable bit 0 in register 05h. This enables hardware generation of SOF.
4. Set the ARM bit at address 00h. This starts the SOF generation.

Table 19. CLM811HST-AXC Slave Mode Registers

Register Name	Endpoint specific register addresses							
	EP 0 – A	EP 0 - B	EP 1 – A	EP 1 - B	EP 2 - A	EP 2 - B	EP 3 - A	EP 3 - B
EP Control Register	00h	08h	10h	18h	20h	28h	30h	0x38
EP Base Address Register	01h	09h	11h	19h	21h	29h	31h	0x39
EP Base Length Register	02h	0Ah	12h	1Ah	22h	2Ah	0x32	0x3A
EP Packet Status Register	03h	0Bh	13h	1Bh	23h	2Bh	0x33	0x3B
EP Transfer Count Register	04h	0Ch	14h	1Ch	24h	2Ch	0x34	0x3C
Register Name		**Miscellaneous register addresses**						
Control Register 1	05h	Interrupt Status Register		0Dh				
Interrupt Enable Register	06h	Current Data Set Register		0Eh				
USB Address Register	07h	Control Register 2		0Fh				
SOF Low Register (read only)	15h	Reserved		1Dh1Fh				
SOF High Register (read only)	16h	Reserved		25h-27h				
Reserved	17h	Reserved		2Dh-2Fh				
DMA Total Count Low Register	35h							
DMA Total Count High Register	36h							
Reserved	37h							
Memory Buffer	40h–FFh							

When in slave mode, the registers in the CLM811HST-AXC are divided into two major groups. The first group contains Endpoint regis- ters that manage USB control transactions and data flow. The second group contains the USB Registers that provide the con- trol and status information for all other operations.

Endpoint Registers

Communication and data flow on USB is implemented using endpoints. These uniquely identifiable entities are the terminals of communication flow between a USB host and USB devices. Each USB device is composed of a collection of independently operating endpoints. Each endpoint has a unique identifier, which is the Endpoint Number. For more information, see USB Specification 1.1 section 5.3.1.

The CLM811HST-AXC supports four endpoints numbered 0–3. Endpoint 0 is the default pipe and is used to initialize and generically manipulate the device to configure the logical device as the Default Control Pipe. It also provides access to the device's configuration information, allows USB status and control access, and supports control transfers.

Endpoints 1–3 support Bulk, Isochronous, and Interrupt transfers. Endpoint 3 is supported by DMA. Each endpoint has two sets of registers—the 'A' set and the 'B' set. This allows overlapped operation where one set of parameters is set up and the other is transferring. Upon completion of a transfer to an endpoint, the 'next data set' bit indicates whether set 'A' or set 'B' is used next. The 'armed' bit of the next data set indicates whether the CLM811HST-AXC is ready for the next transfer without inter- ruption.

Endpoints 0–3 Register Addresses

Each endpoint set has a group of five registers that are mapped within the CLM811HST-AXC memory. The register sets have address assignments Endpoint 0–3 Register Addresses as shown inthe following table.

Table 20. Endpoint 0–3 Register Addresses

Endpoint Register Set	Address (in Hex)
Endpoint 0 – a	00 - 04
Endpoint 0 – b	08 - 0C
Endpoint 1 – a	10 - 14
Endpoint 1 – b	18 - 1C
Endpoint 2 – a	20 - 24
Endpoint 2 – b	28 - 2C
Endpoint 3 – a	30 - 34
Endpoint 3 – b	38 - 3C

For each endpoint set (starting at address Index = 0), the registers are mapped as shown in the following table.

Table 21. Endpoint Register Indices

Endpoint Register Sets (for Endpoint *n* starting at register position *Index=0*)	
Index	Endpoint *n* Control
Index + 1	Endpoint *n* Base Address
Index + 2	Endpoint *n* Base Length
Index + 3	Endpoint *n* Packet Status
Index + 4	Endpoint *n* Transfer Count

Endpoint Control Registers

Endpoint n Control Register [Address a = (EP# * 10h), b = (EP# * 10h)+8]. Each endpoint set has a Control register defined as follows:

Table 22. Endpoint Control Register [Address EP0a/b:00h/08h, EP1a/b:10h/18h, EP2a/b:20h/28h, EP3a/b:30h/38h]

7	6	5	4	3	2	1	0
Reserved	Sequence	Send STALL	ISO	Next Data Set	Direction	Enable	Arm

Bit Position	Bit Name	Function
7	Reserved	
6	Sequence	Sequence bit. ‘0’ if DATA0, ‘1’ if DATA1.
5	Send STALL	When set to ‘1’, sends Stall in response to next request on this endpoint.
4	ISO	When set to ‘1’, allows Isochronous mode for this endpoint.
3	Next Data Set	'0' if next data set is ‘A’, ‘1’ if next data set is 'B'.
2	Direction	When Direction = ‘1’, transmit to Host (IN). When Direction = ‘0’, receive from Host (OUT).
1	Enable	When Enable = ‘1’, allows transfers for this endpoint. When set to ‘0’, USB transactions are ignored. If Enable = ‘1’ and Arm = ‘0’, the endpoint returns NAKs to USB transmissions.
0	Arm	Allows enabled transfers when set = ‘1’. Clears to ‘0’ when transfer is complete.

Endpoint Base Address [Address a = (EP# * 10h)+1, b = (EP# * 10h)+9]]. Pointer to memory buffer location for USB reads and writes.

Table 23. Endpoint Base Address Reg [Address; EP0a/b:01h/09h, EP1a/b:11h/19h, EP2a/b:21h/29h, EP3a/b:31h/39h]

7	6	5	4	3	2	1	0
EPxADD7	EPxADD6	EPxADD5	EPxADD4	EPxADD3	EPxADD2	EPxADD1	EPxADD0

Endpoint Base Length [Address a = (EP# * 10h)+2, b = (EP# * 10h)+A]. The Endpoint Base Length is the maximum packet size for IN/OUT transfers with the host. Essentially, this designates the largest packet size that is received by the CLM811HST-AXC with an OUT transfer, or it designates the size of the data packet sent to the host for IN transfers.

Table 24. Endpoint Base Length Reg [Address EP0a/b:02h/0Ah, EP1a/b:12h/1Ah, EP2a/b:22h/2Ah, EP3a/b:32h/3Ah]

7	6	5	4	3	2	1	0
EPxLEN7	EPxLEN6	EPxLEN5	EPxLEN4	EPxLEN3	EPxLEN2	EPxLEN1	EPxLEN0

Endpoint Packet Status [Address a = (EP# * 10h)+3, b = (EP# * 10h)+Bh]. The packet status contains information relative to the packet that is received or transmitted. The register is defined as follows:

Table 25. Endpoint Packet Status Reg [Address EP0a/b:03h/0Bh, EP1a/b:13h/1Bh, EP2a/b:23h/2Bh, EP3a/b:33h/3Bh]

7	6	5	4	3	2	1	0
Reserved	Reserved	Overflow	Setup	Sequence	Time-out	Error	ACK

Bit Position	Bit Name	Functi on
7	Reserved	Not applicable.
6	Reserved	Not applicable.
5	Overflow	Overflow condition - maximum length exceeded during receives. This is considered a serious error. The maximum number of bytes that can be received by an endpoint is determined by the Endpoint Base Length register for each endpoint. The Overflow bit is only relevant during OUT Tokens from the host.
4	Setup	'1' indicates Setup Packet. If this bit is set, the last packet received was a setup packet.
3	Sequence	This bit indicates if the last packet was a DATA0 (0) or DATA1 (1).
2	Time-out	This bit is not used in slave mode.
1	Error	Error detected in transmission, this includes CRC5/16 and PID errors.
0	ACK	Transmission Acknowledge.

Endpoint Transfer Count [Address a = (EP# * 10h)+4, b = (EP# * 10h)+Ch]. As a peripheral device, the Endpoint Transfer Count register is only important with OUT tokens (host sending the slave data). When a host sends the peripheral data, the Transfer Count register contains the difference between the Endpoint Base Length and the actual number of bytes received in the last packet. In other words, if the Endpoint Base Length register was set for 64 (40h) bytes and an OUT token was sent to the endpoint that only had 16 (10h) bytes, the Endpoint Transfer Count register has a value of 48 (30h). If more bytes were sent in an OUT token then the Endpoint Base Length register was programmed for, the overflow flag is set in the Endpoint Packet Status register and is considered a serious error.

Table 26. Endpoint Transfer Count Reg [Address EP0a/b:04h/0Ch, EP1a/b:14h/1Ch, EP2a/b:24h/2Ch, EP3a/b:34h/3Ch]

7	6	5	4	3	2	1	0
EPxCNT7	EPxCNT6	EPxCNT5	EPxCNT4	EPxCNT3	EPxCNT2	EPxCNT1	EPxCNT0

USB Control Registers

The USB Control registers manage communication and data flow on the USB. Each USB device is composed of a collection of independently operating endpoints. Each endpoint has a unique identifier, which is the Endpoint Number. For more details about USB endpoints, refer to the USB Specification 1.1, Section 5.3.1.

The Control and Status registers are mapped as follows:

Table 27. USB Control Registers

Register Name	Address (in Hex)
Control Register 1	05h
Interrupt Enable Register	06h
USB Address Register	07h
Interrupt Status Register	0Dh
Current Data Set Register	0Eh
Control Register 2	0Fh
SOF Low Byte Register	15h
SOF High Byte Register	16h
DMA Total Count Low Byte Register	35h
DMA Total Count High Byte Register	36h

Control Register 1, Address [05h]. The Control register enables or disables USB transfers and DMA operations with control bits.

Table 28. Control Register 1 [Address 05h]

7	6	5	4	3	2	1	0
Reserved	STBYD	SPSEL	J-K1	J-K0	DMA Dir	DMA Enable	USB Enable

Bit Position	Bit Name	Function
7	Reserved	Reserved bit - must be set to '0'.
6	STBYD	XCVR Power Control. ‘1’ sets XCVR to low power. For normal operation set this bit to ‘0’. Suspend mode is entered if bit 6 = ‘1’ and bit ‘0’ (USB Enable) = ‘0’.
5	SPSEL	Speed Select. ‘0’ selects full speed. ‘1’ selects low speed (also see Table 33 on page 20).
4	J-K Force State	J-K1 and J-K0 force state control bits are used to generate various USB bus conditions. Forcing K-state is used for Peripheral device remote wake-up, Resume, and other modes. These two bits are set to zero on power-up, see Table 12 on page 11 for functions.
3	USB Engine Reset	
2	DMA Dir	DMA Transfer Direction. Set equal to ‘1’ for DMA READ cycles from CLM811HST-AXC. Set equal to ‘0’ for DMA WRITE cycles.
1	DMA Enable	Enable DMA operation when equal to ‘1’. Disable = ‘0’. DMA is initiated when DMA Count High is written.
0	USB Enable	Overall Enable for Transfers. ‘1’ enables and’ ‘0 disables. Set this bit to ‘1’ to enable USB communication. Default at power-up = ‘0’

JK-Force State	USB Engine Reset	Function
0	0	Normal operating mode
0	1	Force SE0, D+ and D– are set low
1	0	Force K-State, D– set high, D+ set low
1	1	Force J-State, D+ set high, D– set low

Interrupt Enable Register, Address [06h] . The CLM811HST-AXC provides an Interrupt Request Output that is activated resulting from a number of conditions. The Interrupt Enable register allows the user to select events that generate the Interrupt Request Output assertion. A separate Interrupt Status register is read in order to determine the condition that initiated the interrupt (see the description in section Interrupt Status Register, Address [0Dh]). When a bit is set to ‘1’, the corresponding interrupt is enabled. Setting a bit in the Interrupt Enable register does not effect the Interrupt Status register’s value; it just determines which interrupts are output on INTRQ.

Table 29. Interrupt Enable Register [Address: 06h]

7	6	5	4	3	2	1	0
DMA Status	USB Reset	SOF Received	DMA Done	Endpoint 3 Done	Endpoint 2 Done	Endpoint 1 Done	Endpoint 0 Done

Bit Position	Bit Name	Function
7	DMA Status	When equal to ‘1’, indicates DMA transfer is in progress. When equal to ‘0’, indicates DMA transfer is complete.
6	USB Reset	Enable USB Reset received interrupt when = ‘1’.
5	SOF Received	Enable SOF Received Interrupt when = ‘1’.
4	DMA Done	Enable DMA done Interrupt when = ‘1’.
3	Endpoint 3 Done	Enable Endpoint 3 done Interrupt when = ‘1’.
2	Endpoint 2 Done	Enable Endpoint 2 done Interrupt when = ‘1’.
1	Endpoint 1 Done	Enable Endpoint 1 done Interrupt when = ‘1’.
0	Endpoint 0 Done	Enable Endpoint 0 done Interrupt when = ‘1’.

USB Address Register, Address [07h]

This register contains the USB Device Address after assignment by USB host during configuration. On power-up or reset, USB Address register is set to Address 00h. After USB configuration and address assignment, the device recognizes only USB transactions directed to the address contained in the USB Address register.

Table 30. USB Address Register [Address 07h]

7	6	5	4	3	2	1	0
USBADD7	USBADD6	USBADD5	USBADD4	USBADD3	USBADD2	USBADD1	USBADD0

Interrupt Status Register, Address [0Dh]

This read/write register serves as an Interrupt Status register when it is read, and an Interrupt Clear register when it is written. To clear an interrupt, write the register with the appropriate bit set to ‘1’. Writing a ‘0’ has no effect on thestatus.

Table 31. Interrupt Status Register [Address 0Dh]

7	6	5	4	3	2	1	0
DMA Status	USB Reset	SOF Received	DMA Done	Endpoint 3 Done	Endpoint 2 Done	Endpoint 1 Done	Endpoint 0 Done

Bit Position	Bit Name	Function
7	DMA Status	When equal to ‘1’, indicates DMA transfer is in progress. When equal to 0, indicates DMA transfer is complete. An interrupt is not generated when DMA is complete.
6	USB Reset	USB Reset Received Interrupt.
5	SOF Received	SOF Received Interrupt.
4	DMA Done	DMA Done Interrupt.
3	Endpoint 3 Done	Endpoint 3 Done Interrupt.
2	Endpoint 2 Done	Endpoint 2 Done Interrupt.
1	Endpoint 1 Done	Endpoint 1 Done Interrupt.
0	Endpoint 0 Done	Endpoint 0 Done Interrupt.

Current Data Set Register, Address [0Eh]. This register indicates current selected data set for each endpoint.

Table 32. Current Data Set Register [Address 0Eh]

7	6	5	4	3	2	1	0
Reserved				Endpoint 3	Endpoint 2	Endpoint 1	Endpoint 0

Bit Position	Bit Name	Function
7–4	Reserved	Not applicable.
3	Endpoint 3 Done	Endpoint 3a = 0, Endpoint 3b = 1.
2	Endpoint 2 Done	Endpoint 2a = 0, Endpoint 2b = 1.
1	Endpoint 1 Done	Endpoint 1a = 0, Endpoint 1b = 1.
0	Endpoint 0 Done	Endpoint 0a = 0, Endpoint 0b = 1.

Control Register 2, Address [0Fh]. Control Register 2 is used to control if the device is configured as a master or a slave. It can change the polarity of the Data+ and Data- pins to accommodate both full- and low speed operation.

Table 33. Control Register 2 [Address 0Fh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLM811HST-AXC Master/ Slave selection	CLM811HST-AXC D+/D– Data Polarity Swap	Reserved					

Bit Position	Bit Name	Function
7	CLM811HST-AXC Master/ Slave selection	Master = ‘1’ Slave = ‘0’
6	CLM811HST-AXC D+/D– Data Polarity Swap	’1’ = change polarity (low speed) ’0’ = no change of polarity (full speed)
5–0	Reserved	NA

SOF Low Register, Address [15h]. Read only register contains the 7 low order bits of Frame Number in positions: bit 7:1. Bit 0 is undefined. Register is updated when a SOF packet is received. Do not write to this register.

SOF High Register, Address [16h]. Read only register contains the 4 low order bits of Frame Number in positions: bit 7:4. Bits 3:0 are undefined and should be masked when read by the user. This register is updated when a SOF packet is received. The user should not write to this register.

DMA Total Count Low Register, Address [35h]. The DMA Total Count Low register contains the low order 8 bits of DMA count. DMA total count is the total number of bytes to be transferred between a peripheral to the CLM811HST-AXC. The count may sometimes require up to 16 bits, therefore the count is represented in two registers: Total Count Low and Total Count High. EP3 is only supported with DMA operation.

DMA Total Count High Register, Address [36h]. The DMA Total Count High register contains the high order 8 bits of DMA count. When written, this register enables DMA if the DMA Enable bit is set in Control Register 1. The user should always write Low Count register first, followed by a write to High Count register, even if high count is 00h.

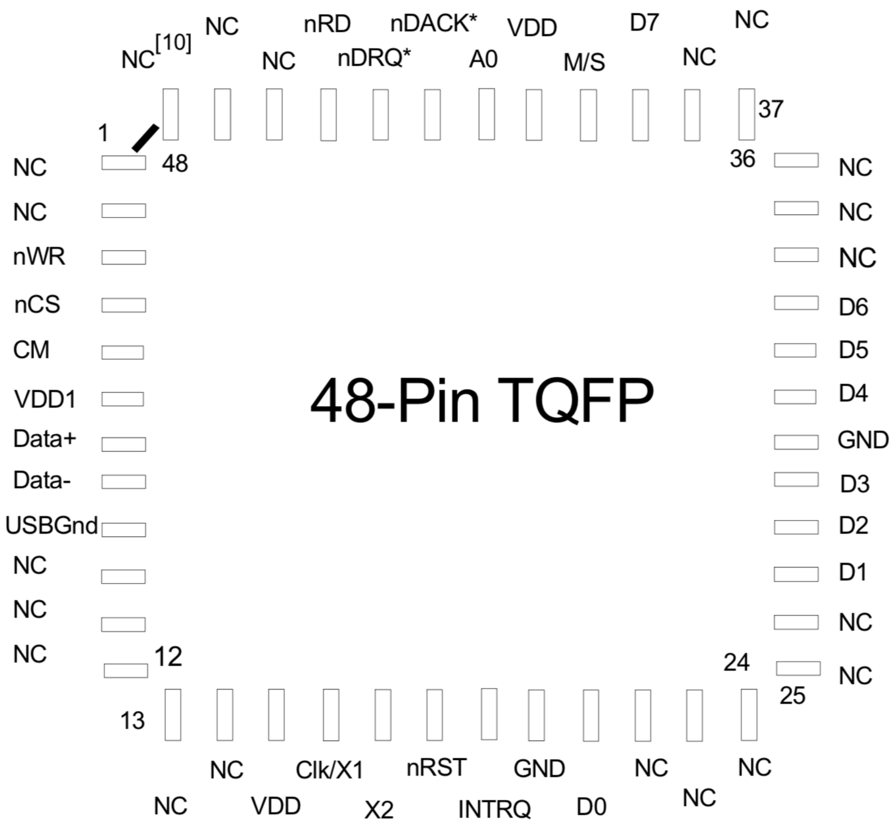
Physical Connections

These parts are offered in 48-pin TQFP package. The 48-pin TQFP package is the CLM811HST-AXC.

48-Pin TQFP Physical Connections

48-Pin TQFP AXC Pin Layout

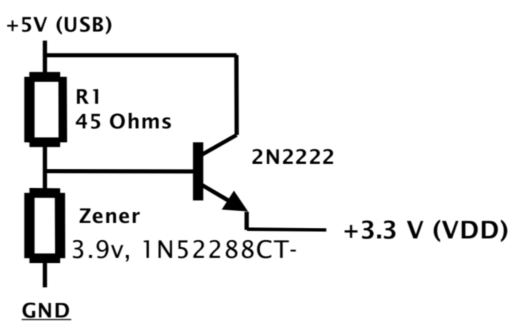
Figure 4. 48-pin TQFP AXC USB Host/Slave Controller Pin Layout



*See Table 34 on page 22 for Pin and Signal Description for Pins 43 and 44 in Host Mode.

The diagram below illustrates a simple +3.3 V voltage source.

Figure 5. Sample VDD Generator



USB Host Controller Pins Description

The CLM811HST-AXC is packaged in a 48-pin TQFP. These devices require a 3.3 VDC power source and an external 12 or 48 MHz crystal or clock.

Table 34. Pin and Signal Description for Pins

48-Pin TQFP AXC Pin No.	Pin Type	Pin Name	Pin Description
1	NC	NC	No connection.
2	NC	NC	No connection.
3	IN	nWR	**Write Strobe Input**. An active LOW input used with nCS to write to registers/data memory.
4	IN	nCS	**Active LOW 48-Pin TQFP Chip select**. Used with nRD and nWr when accessing the 48-Pin TQFP.
5[11]	IN	CM	**Clock Multiply**. Select 12 MHz/48 MHz Clock Source.
6	VDD1	+3.3 VDC	**Power for USB Transceivers**. V_{DD1} may be connected to V_{DD}.
7	BIDIR	DATA +	USB Differential Data Signal HIGH Side.
8	BIDIR	DATA -	USB Differential Data Signal LOW Side.
9	GND	USB GND	Ground Connection for USB.
10	NC	NC	No connection.
11	NC	NC	No connection.
12	NC	NC	No connection.
13	NC	NC	No connection.
14	NC	NC	No connection.
15[12]	VDD	+3.3 VDC	Device V_{DD} Power.
16	IN	CLK/X1	Clock or External Crystal X1 connection. The X1/X2 Clock requires external 12 or 48 MHz matching crystal or clock source.
17	OUT	X2	External Crystal X2 connection.
18	IN	nRST	Device active low reset input.
19	OUT	INTRQ	Active HIGH Interrupt Request output to external controller.
20	GND	GND	Device Ground.
21	BIDIR	D0	**Data 0**. Microprocessor Data/Address Bus.
22	NC	NC	No connection.
23	NC	NC	No connection.
24	NC	NC	No connection.
25	NC	NC	No connection.
26	NC	NC	No connection.
27	BIDIR	D1	**Data 1**. Microprocessor Data/Address Bus.
28	BIDIR	D2	**Data 2**. Microprocessor Data/Address Bus.
29	BIDIR	D3	**Data 3**. Microprocessor Data/Address Bus.
30	GND	GND	Device Ground.
31	BIDIR	D4	**Data 4**. Microprocessor Data/Address Bus.
32	BIDIR	D5	**Data 5**. Microprocessor Data/Address Bus.

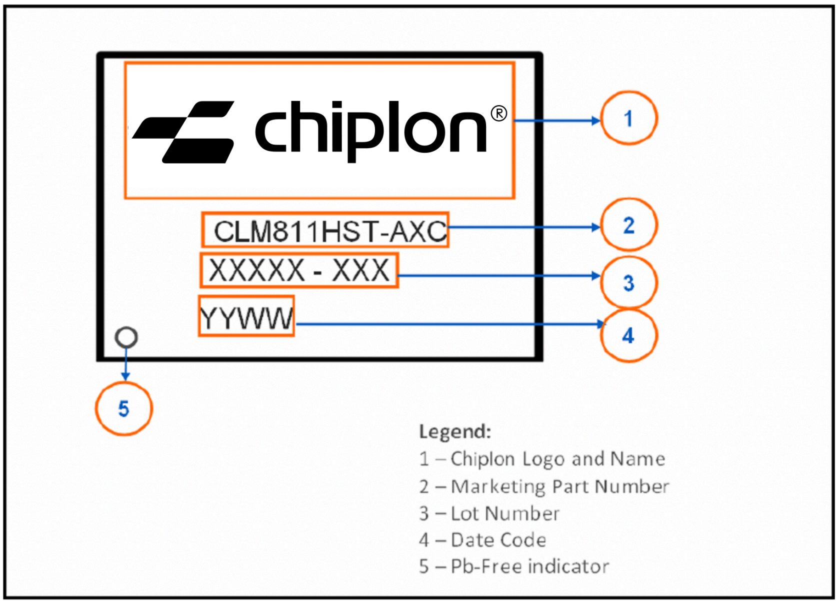
Notes

11. The CM Clock Multiplier pin must be tied HIGH for a 12 MHz clock source and tied to ground for a 48 MHz clock source.
12. VDD can be derived from the USB supply. See Figure 5 on page 21.

Table 34. Pin and Signal Description for Pins

48-Pin TQFP AXC Pin No.	Pin Type	Pin Name	Pin Description
33	BIDIR	D6	**Data 6**. Microprocessor Data/Address Bus.
34	NC	NC	No connection.
35	NC	NC	No connection.
36	NC	NC	No connection.
37	NC	NC	No connection.
38	NC	NC	No connection.
39	BIDIR	D7	**Data 7**. Microprocessor Data/Address Bus.
40	IN	M/S	**Master/Slave Mode Select**. ‘1’ selects Slave. ‘0’ = Master.
41	VDD	+3.3 VDC	Device V_{DD} Power.
42[14]	IN	A0	**A0 = ‘0’.** Selects address pointer. Register A0 = ‘1’. Selects data buffer or register.
43	IN	nDACK	**DMA Acknowledge**. An active LOW input used to interface to an external DMA controller. DMA is enabled only in slave mode. In host mode, the pin should be tied HIGH (logic ‘1’).
44	OUT	nDRQ	**DMA Request**. An active LOW output used with an external DMA controller. nDRQ and nDACK form the handshake for DMA data transfers. In host mode, leave the pin unconnected.
45	IN	nRD	**Read Strobe Input**. An active LOW input used with nCS to read registers/data memory.
46	NC	NC	No connection.
47	NC	NC	No connection.
48	NC	NC	No connection.

Figure 6. Package Markings (48-Pin TQFP)



Electrical Specifications

Absolute Maximum Ratings

This section lists the absolute maximum ratings of the CLM811HST-AXC. Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Description	Condition
Storage Temperature	–40 °C to 125 °C
Voltage on any pin with respect to ground	–0.3 V to 6.0 V
Power Supply Voltage (V_{DD})	4.0 V
Power Supply Voltage (V_{DD1})	4.0 V
Lead Temperature (10 seconds)	180°C

Recommended Operating Conditions

Parameter	Min	Typical	Max
Power Supply Voltage, VDD	3.0 V	3.3 V	3.45 V
Power Supply Voltage, VDD1	3.0 V		3.45 V
Operating Temperature	0 °C		65 °C

Crystal Requirements, (X1, X2)	Min	Typical	Max
Operating Temperature Range	0°C		65 °C
Parallel Resonant Frequency		48 MHz	
Frequency Drift over Temperature			±50 ppm
Accuracy of Adjustment			±30 ppm
Series Resistance			100 Ohms
Shunt Capacitance	3 pF		6 pF
Load Capacitance		20 pF	
Drive Level	20 μW		5 mW
Mode of Vibration Third Overtone[15]			

External Clock Input Characteristics (X1)

Parameter	Min	Typical	Max
Clock Input Voltage at X1 (X2 Open)	1.5 V		
Clock Frequency[16]		48 MHz	

Notes
15. Fundamental mode for 12 MHz Crystal.
16. The CLM811HST-AXC can use a 12 MHz Clock Source.

DC Characteristics

Parameter	Description	Min	Typ	Max
V_{IL}	Input Voltage LOW	–0.3 V		0.8 V
V_{IH}	Input Voltage HIGH (5 V Tolerant I/O)	2.0 V		6.0 V
V_{OL}	Output Voltage LOW (I_{OL} = 4 mA)			0.4 V
V_{OH}	Output Voltage HIGH (I_{OH} = –4 mA)	2.4 V		
I_{OH}	Output Current HIGH	4 mA		
I_{OL}	Output Current LOW	4 mA		
I_{LL}	Input Leakage			±1 µA
C_{IN}	Input Capacitance			10 pF
I_{CC}[17]	Supply Current (V_{DD}) inc USB at FS		21 mA	25 mA
I_{CCsus1}[18]	Supply Current (V_{DD}) Suspend w/Clk & Pll Enb		4.2 mA	5 mA
I_{CCsus2}[19]	Supply Current (V_{DD}) Suspend no Clk & Pll Dis		50 µA	60 µA
I_{USB}	Supply Current (V_{DD1})			10 mA
I_{USBSUS}	Transceiver Supply Current in Suspend			10 µA

USB Host Transceiver Characteristics

Parameter	Description	Min	Typ[20]	Max
V_{IHYS}	Differential Input Sensitivity (Data+, Data–)	0.2 V		200 mV
V_{USBIH}	USB Input Voltage HIGH Driven	2.0 V		
V_{USBIL}	USB Input Voltage LOW	0.8 V		
V_{USBOH}	USB Output Voltage HIGH	2.0 V		
V_{USBOL}	USB Output Voltage LOW	0.0 V		0.3 V
Z_{USBH}[21]	Output Impedance HIGH STATE	36 Ohms		42 Ohms
Z_{USBL}[21]	Output Impedance LOW STATE	36 Ohms		42 Ohms
I_{USB}	Transceiver Supply p-p Current (3.3 V)			10 mA at FS

Every V_{DD} pin, including USB V_{DD}, must have a decoupling capacitor to ensure clean V_{DD} (free of high frequency noise) at the chip input point (pin) itself.

The best way to do this is to connect a ceramic capacitor (0.1 µF, 6 V) between the pin itself and a good ground. Keep capacitor leads as short as possible. Use surface mount capacitors with the shortest traces possible (the use of a ground plane is strongly recom- mended).

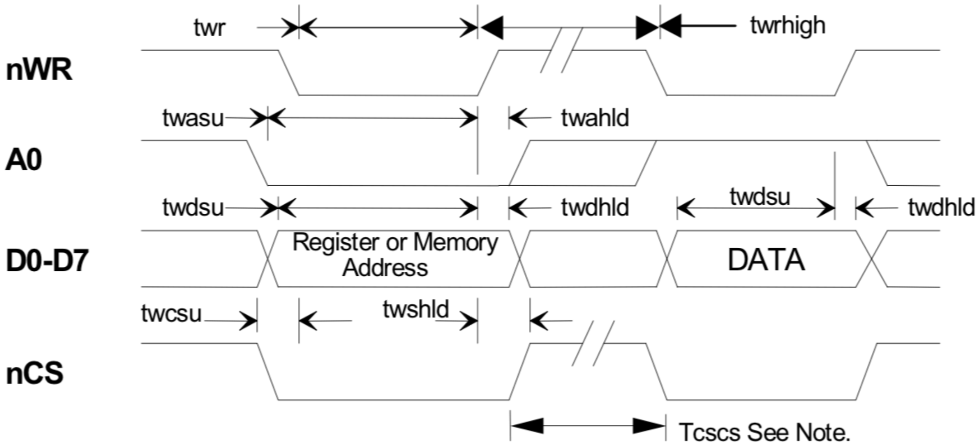
This product was tested as compliant to the USB-IF specification under the test identification number (TID) of 40000689 and is listed on the USB-IF's integrators list.

Notes

17. I_{CC} measurement includes USB Transceiver current (I_{USB}) operating at full speed.
18. I_{CCsus1} measured with 12 MHz Clock Input and Internal PLL enabled. Suspend set –(USB transceiver and internal Clocking disabled).
19. I_{CCsus2} measured with external Clock, PLL disabled, and Suspend set. For absolute minimum current consumption, ensure that all inputs to the device are at static logic level.
20. All typical values are V_{DD} = 3.3 V and T_{AMB}= 25°C.
21. Z_{USBX} impedance values includes an external resistor of 24 Ohms ± 1% (CLM811HST-AXC revision 1.2 requires external resistor values of 33 Ohms ±1%).

Bus Interface Timing Requirements

I/O Write Cycle

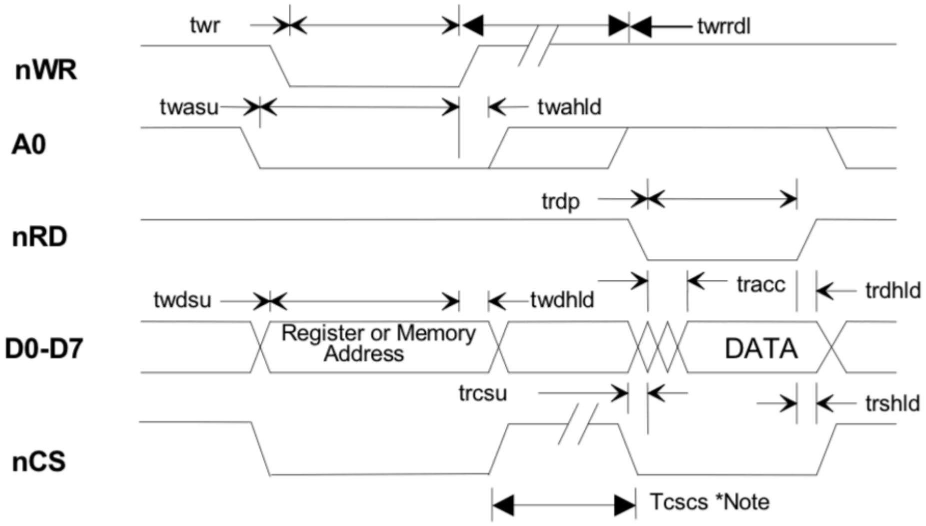


I/O Write Cycle to Register or Memory Buffer

Parameter	Description	Min	Typ	Max
t_{WR}	Write pulse width	85 ns		
t_{WCSU}	Chip select set-up to nWR LOW	0 ns		
t_{WSHLD}	Chip select hold time After nWR HIGH	0 ns		
t_{WASU}	A0 address setup time	85 ns		
t_{WAHLD}	A0 address hold time	10 ns		
t_{WDSU}	Data to Write HIGH set-up time	85 ns		
t_{WDHLD}	Data hold time after Write HIGH	5 ns		
t_{CSCS}	nCS inactive to nCS* asserted	85 ns		
t_{WRHIGH}	NWR HIGH	85 ns		

Note nCS an be held LOW for multiple Write cycles provided nWR is cycled. Write Cycle Time for Auto Inc Mode Writes is 170 ns minimum.

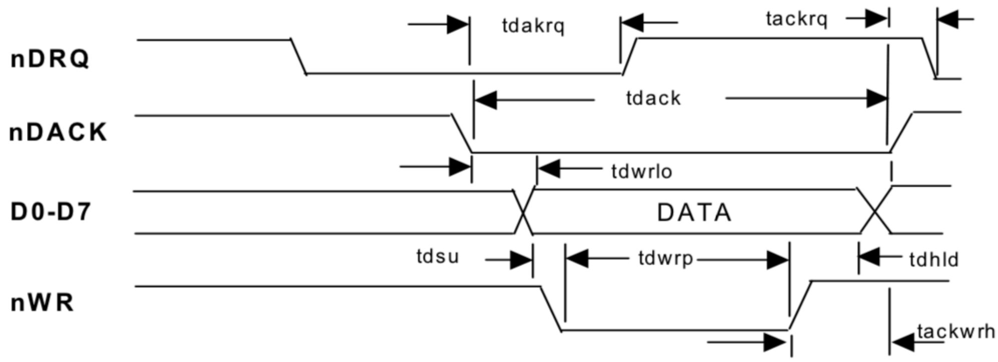
I/O Read Cycle



I/O Read Cycle from Register or Memory Buffer

Parameter	Description	Min	Typ	Max
t_{WR}	Write pulse width	85 ns		
t_{RD}	Read pulse width	85 ns		
t_{WCSU}	Chip select set-up to nWR	0 ns		
t_{WASU}	A0 address set-up time	85 ns		
t_{WAHLD}	A0 address hold time	10 ns		
t_{WDSU}	Data to Write HIGH set-up time	85 ns		
t_{WDHLD}	Data hold time after Write HIGH	5 ns		
t_{RACC}	Data valid after Read LOW	25 ns		85 ns
t_{RDHLD}	Data hold after Read HIGH	40 ns		
t_{RCSU}	Chip select LOW to Read LOW	0 ns		
t_{RSHLD}	NCS hold after Read HIGH	0 ns		
T_{CSCS}*	nCS inactive to nCS *asserted	85 ns		
t_{WRRDL}	nWR HIGH to nRD LOW	85ns		

Note nCS can be kept LOW during multiple Read cycles provided nRD is cycled. Rd Cycle Time for Auto Inc Mode Reads is 170 ns minimum.

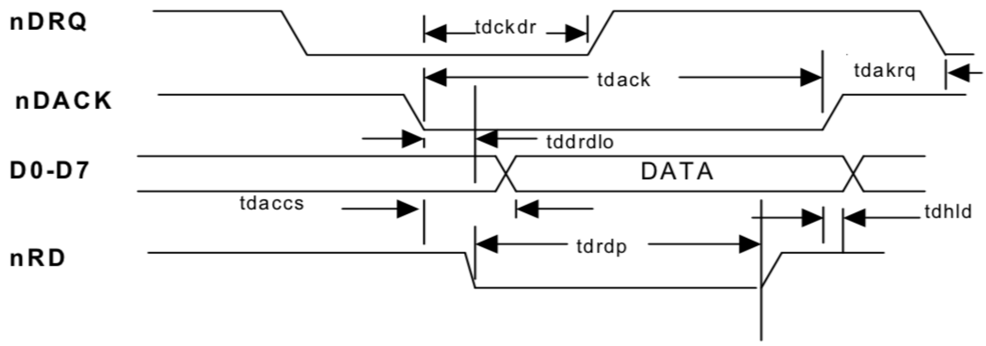


DMA Write Cycle

Parameter	Descripti on	Min	Typ	Max
tdack	nDACK low	80 ns		
tdwrlo	nDACK to nWR low delay	5 ns		
tdakrq	nDACK low to nDRQ high delay	5 ns		
tdwrp	nWR pulse width	65 ns		
tdhld	Data hold after nWR high	5 ns		
tdsu	Data set-up to nWR strobe low	60 ns		
tackrq	NDACK high to nDRQ low	5 ns		
tackwrh	NDACK high to nDRQ low	5 ns		
twrcycle	DMA Write Cycle Time	150 ns		

Note nWR must go low after nDACK goes low in order for nDRQ to clear. If this sequence is not implemented as requested, the next nDRQ is not inserted.

DMA Read Cycle

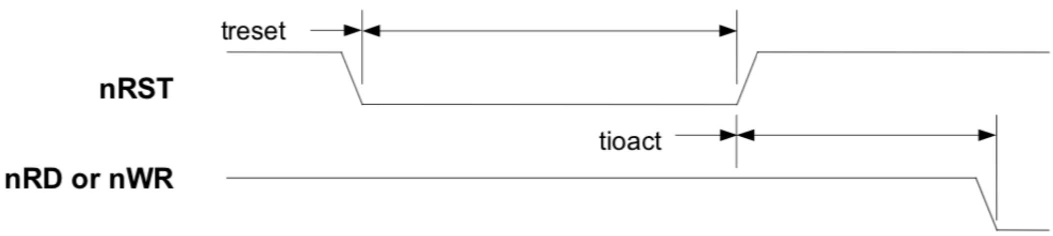


CLM811 **DMA Read Cycle Timing**

Parameter	Description	Min	Typ	Max
tdack	nDACK low	100 ns		
tddrdlo	nDACK to nRD low delay	0 ns		
tdckdr	nDACK low to nDRQ high delay	5 ns		
tdrdp	nRD pulse width	90 ns		
tdhld	Date hold after nDACK high	5 ns		
tddaccs	Data access from nDACK low	85 ns		
tdrdack	nRD high to nDACK high	0 ns		
tdakrq	nDRQ low after nDACK high	5 ns		
trdcycle	DMA Read Cycle Time	150 ns		

Note Data is held until nDACK goes high regardless of state of nREAD.

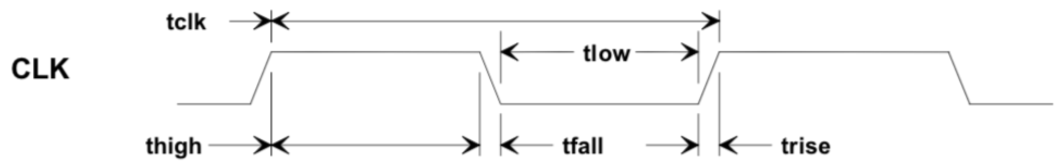
Reset Timing



Reset Timing

Parameter	Description	Min	Typ	Max
t_{RESET}	nRst Pulse width	16 clocks		
t_{IOACT}	nRst HIGH to nRD or nWR active	16 clocks		

Note Clock is 48 MHz nominal.



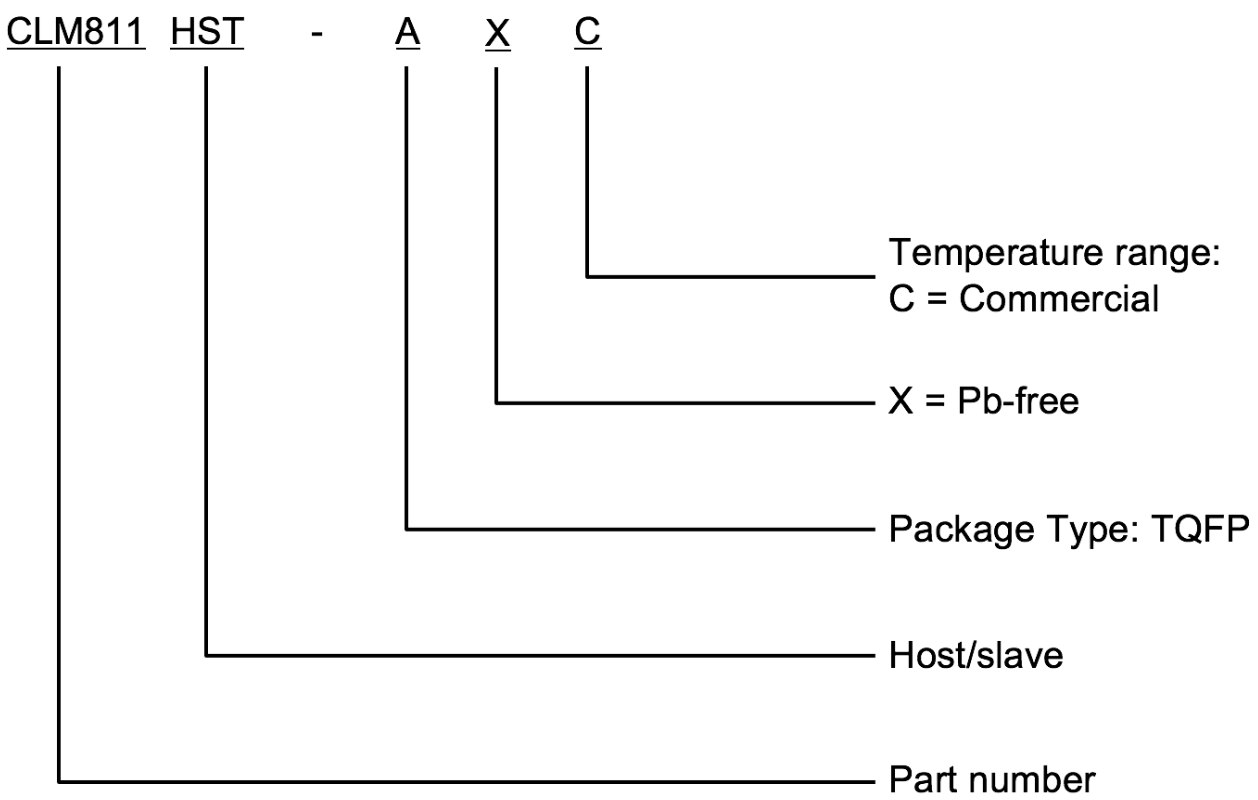
Clock Timing

Parameter	Description	Min	Typ	Max
t_{CLK}	Clock Period (48 MHz)	20.0 ns	20.8 ns	
t_{HIGH}	Clock HIGH Time	9 ns		11 ns
t_{LOW}	Clock LOW Time	9 ns		11 ns
t_{RISE}	Clock Rise Time			5.0 ns
t_{FALL}	Clock Fall Time			5.0 ns
	Clock Duty Cycle	45%		55%

Ordering Information

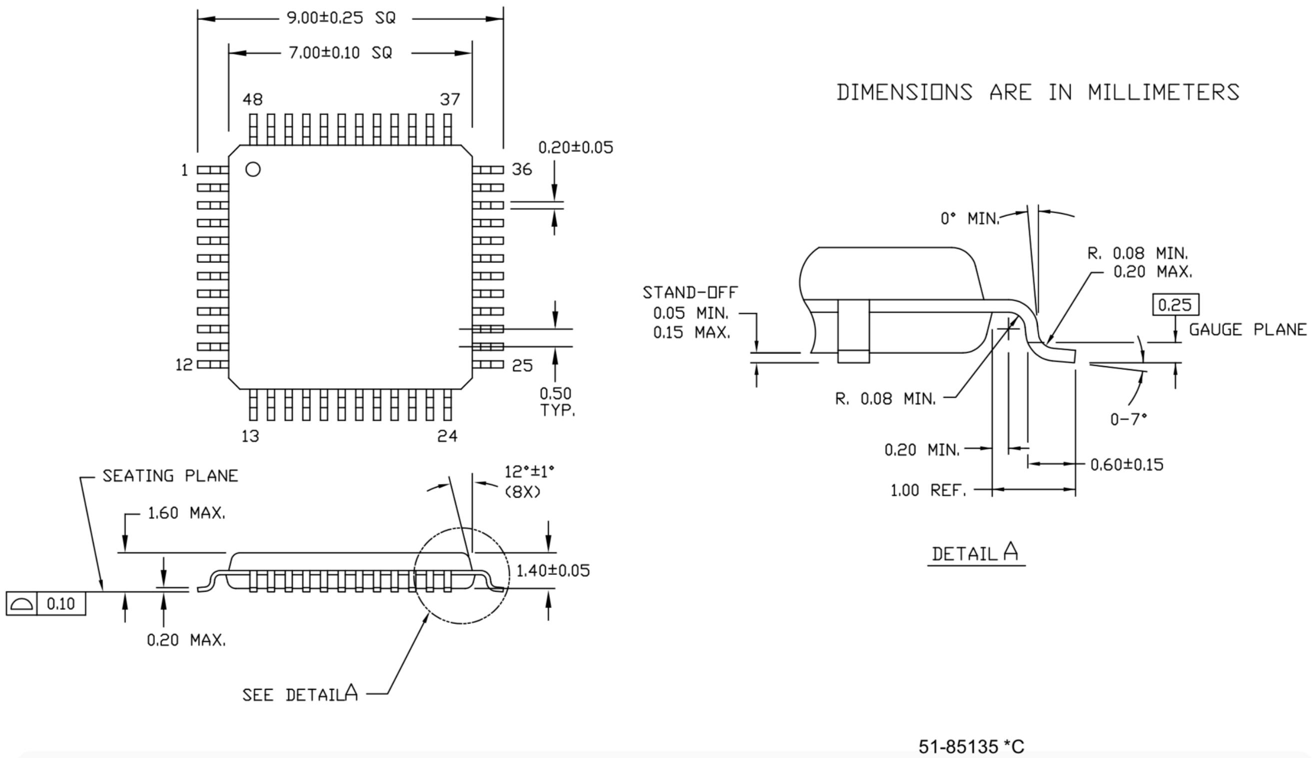
Part Number	Package Type	
CLM811HST-AXC	48-pin Pb-free	–

Ordering Code Definitions



Package Diagram

Figure 7. 48-pin TQFP (7 × 7 × 1.4 mm) Package Outline, 51-85135



Acronyms

Table 35. Acronyms Used in this Document

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CRC	Cyclical Redundancy Check
DMA	Direct Memory Access
DPLL	Dynamic Phase Locked Loop
I/O	Input Output
PCMCIA	Personal Computer Memory Card International Association
RAM	Random Access Memory
SIE	Serial Interface Engine
SOF	Start of Frame
SRAM	Static Random Access Memory
USB	Universal Serial Bus

Document Conventions

Symbol	Unit of Measure
mA	milliampere
Mbps	megabits per second
MHz	megahertz
mV	millivolt
mW	milliwatt
ns	nanosecond
ppm	parts per million
pF	picofarad
V	volt
VDC	volts (direct current)

Errata

This section describes the errata for the CLM811HST-AXC. Details include errata trigger conditions, available workaround, and silicon revision applicability.

Contact your local Chiplon Sales Representative if you have questions.

Part Numbers Affected

Part Number	Package Type	Operating Range
CLM811HS T-AXC	All	Commercial

CLM811HST-AXC/CLM811 Qualification Status

Product status: In production - Qual Report: 014401

CLM811HST-AXC/CLM811 Errata Summary

The following table defines the errata applicability to available CLM811HST-AXC/CLM811 family of devices.

Note Errata titles in this table are hyperlinked. Click an entry to go to its description.

Ite ms	CLM811HST-AXC/CLM811S	Rev Letter/ Number	Fix Status
1. Host Mode: SE0 problem in low-speed hub operation	X	1.5	Use workaround
2. Host Mode: Sync to SOF does not apply to low-speed mode	X	1.5	Use workaround
3. Host/Peripheral Mode: 12 MHz operation with sensitive in- ternal PLL	X	1.5	Use workaround
4. Peripheral Mode: Unreliable DMA interface	X	1.5	Use workaround
5. Peripheral Mode: CLM811HST-AXC can miss packets in a noisy environment	X	1.5	Use workaround
6. Host/Peripheral Mode: Auto-increment feature results in corrupt data	X	1.5	Use workaround

1. Host Mode: SEO problem in low-speed hub operation

- **Problem Definition**

  Some hubs that send SE0s upstream during the EOF1 time frame may cause the CLM811HST-AXC to stop sending SOFs. This problem occurs when operating with low-speed devices attached downstream of such a hub. This is not a problem with full-speed devices. According to the USB Specification, hubs are permitted to transmit SE0s during the EOF1 time frame. This is done to eliminate potential babble conditions on the bus and is an optional feature implemented in some hubs.

- **Parameters Affected**

  SOFs

- **Trigger Condition(S)**

  Attaching hub that sends SE0s upstream during the EOF1 time frame.

- **Scope of Impact**

  The CLM811HST-AXC can not host a low-speed device downstream of a hub that generates SE0s during EOF1.

- **Workaround**

  The only complete workaround is to use a hub that does not transmit SE0s upstream during EOF1. Some hubs, including all Chiplon hubs, have the option to disable SE0s from being generated during EOF1.

  For a list of hubs that do not generate SE0s upstream during EOF1, or for more information on disabling this feature in Chiplon hubs, contact Chiplon USB support.

- **Fix Status**

  Use workaround.

2. Host Mode: Sync to SOF does not apply to low-speed mode

- **Problem Definition**

  The SYNC to SOF bit (bit 5) of the USB Host Control Registers [00H, 08H], is only designed for full-speed support. However, all other full-speed SOF bits and registers do apply to low-speed EOPs as well. In full-speed mode, this bit should only be used when the software cannot fit a packet within the remaining 1 ms frame. Setting this bit automatically delays sending the packet until the next SOF.

- **Parameters Affected**

  SYNC to SOF

- **Trigger Condition(S)**

  Full-speed support.

- **Scope of Impact**

  If the SOF bit is set when operating in low-speed mode, packets may not get sent from the CLM811HST-AXC.

- **Workaround**

  Do not set the SOF bit when operating in low-speed mode. Instead, if a packet does not fit within the remaining 1 ms frame, firmware needs to delay sending it until after the next EOP. Using a simple delay loop or using the SOF timer interrupt (also EOP timer interrupt in low-speed mode) are two possible ways of doing this.

- **Fix Status**

  Use workaround.

3. Host/Peripheral Mode: 12 MHz operation with sensitive internal PLL

- **Problem Definition**

  The internal PLL is very sensitive. The PLL causes any high frequency noise on the V_{DD} pins to result in clock jitter.

- **Parameters Affected**

  USB data signaling at full-speed and improper timing of SOF packets.

- **Trigger Condition(S)**

  Operation at 12 MHz with high frequency noise on the V_{DD} pins.

- **Scope of Impact**

  When operating the CLM811HST-AXC at 12 MHz, high frequency noise on the V_{DD} pins can result in clock jitter. The clock jitter results in different symptoms depending on the severity of the jitter. Most notable is improper USB data signaling at full speed and improper timing of SOF packets.

- **Workaround**

  The best workaround is to use 48 MHz to eliminate using the PLL. If 12 MHz is required, take these steps to reduce any jitter output of the PLL.

  1. Reduce high frequency noise on all CLM811HST-AXC V_{DD} pins. This can be accomplished by adding proper decoupling capacitors directly on the V_{DD} pins. The value of 0.1 μF can be too large, depending on the inductivity of the traces on the PCB; experiment with values of 0.01 μF or even 1000 pF. In addition, ceramic capacitors are recommended.
  2. Use a 12 MHz oscillator instead of a crystal. An oscillator produces much sharper edge rates, which allow more tolerance for jitter.
  3. Careful layout can minimize this PLL jitter significantly:

  a. Use the shortest traces possible for decoupling capacitors.

  b. Use ground and VCC planes.

- **Fix Status**

  Use workaround.

4. Peripheral Mode: Unreliable DMA interface

- **Problem Definition**

  The DMA interface can be unreliable in slave mode.

- **Parameters Affected**

  DMA transfers to or from the CLM811HST-AXC internal RAM.

- **Trigger Condition(S)**

  Use of the DMA interface to move data to or from CLM811HST-AXC internal RAM.

- **Scope of Impact**

  When performing DMA writes, data may get corrupted. This problem has only been seen for DMA write operations, but can also occur for read operations as well.

- **Workaround**

  Use the standard Data Port interface instead of the DMA interface for writing to or reading from the CLM811HST-AXC RAM space. The DMA interface is not a recommended interface for the CLM811HST-AXC due to this issue.

- **Fix Status**

  Use workaround.

5. Peripheral Mode: CLM811HST-AXC can miss packets in a noisy environment

- **Problem Definition**

  In a noisy environment, the CLM811HST-AXC has the potential to occasionally miss a packet. Occasionally missed packets are anticipated and dealt with in USB 2.0 Specification Section 10.2.6, where the following applies “It is recommended that the error count not be incremented when there is an error due to host specific reasons (buffer underrun or overrun), and that whenever a transaction does not encounter a transmission error, the error count be reset to zero.” In other words if an individual packet is missed and the next packet is processed properly, the recommendation is that the error counter be reset to ‘0’. When drivers are written with this in mind, they can avoid issues that cause the transfer to be retired due to three errors in a transaction.

- **Parameters Affected**

  Error count.

- **Trigger Condition(S)**

  Electrically noisy environments.

- **Scope of Impact**

  If the CLM811HST-AXC is used in an electrically noisy environment that may corrupt three requests within that transaction, the transaction will be retired by the host.

- **Workaround**

  1) The workaround for this issue is to write the driver according to the guidelines specified in section 10.2.6 of the USB 2.0 Specification, to prevent the driver from retrying the transfer.

  2) Board layout is the major reason for electrical noise that can aggravate this issue. When doing layout for the USB chip, use guidelines provided in a Chiplon application note titled, *High-speed USB PCB Layout Recommendations* found on the Chiplon web site.

- **Fix Status**

  Use workaround.

6. Host/Peripheral Mode: Auto-increment feature results in corrupt data

- **Problem Definition**

  The CLM811HST-AXC has a feature called auto-increment used to read or write blocks of the data buffer. This feature is used to speed up the time it takes to write blocks of data because an address location write is not required between data writes or reads. In some cases, the auto-increment feature can intermittently fail, causing the RAM location to be corrupted or the read buffer to provide incorrect data to the system processor. This type of error is very infrequent.

- **Parameters Affected**

  Any RAM location where auto-increment feature is used to access data. This includes both register and buffer space.

- **Trigger Condition(S)**

  Use of the auto-increment feature.

- **Scope of Impact**

  When using the auto-increment feature for writes or reads, it is possible for the data to become corrupt. The following table demonstrates a typical error when it occurs. The error condition is shown in red.

  If an error occurs during writes using auto-increment, an address location can be written with the value of the previous address; each subsequent write will also be incorrect until the end of the block write. In the following example, note that the value of 0x01 from address 0x11 is incorrectly written to address 0x12 instead of the expected value of 0x02. After this error, the write to each subsequent address is also incorrectly written with the value that was intended to be in the previous address location.

  If an error occurs during a read using auto-increment, a single location can be incorrectly read as the previous addresses value. If the data is read again, it will show that the data in RAM is correct.

Auto-increment error during a write								
Address	**0x10**	**0x11**	**0x12**	**0x13**	**0x14**	**......**	**0x1E**	**0x1F**
Data intended to be written to RAM	0x00	0x01	0x02	0x03	0x04	.....	0x0E	0x0F
Data actually written to RAM	0x00	0x01	**0x01**	**0x02**	**0x03**	**.....**	**0x0D**	**0x0E**
Auto-increment error during a read								
Address	**0x10**	**0x11**	**0x12**	**0x13**	**0x14**	**......**	**0x1E**	**0x1F**
Data actually in RAM	0x00	0x01	0x02	0x03	0x04	.....	0x0E	0x0F
Data read back from RAM	0x00	0x01	**0x01**	0x03	0x04	.....	0x0E	0x0F

- **Workaround**

  The easiest way to work around this issue is to not use the auto-increment feature. This affects performance because the address must be written prior to each write or read.

- **Fix Status**

  Use workaround.