CLM4717
4.5Ω/20Ω, 300MHz Bandwidth, Dual SPDT Chiplon Switches in UCSP

General Description

The CLM4717 low-voltage, low on-resistance (R_{ON}), dual single-pole/double throw (SPDT) Chiplon switches operate from a single +1.8V to +5.5V supply. These devices are designed for USB 1.1 and audio switching applications.

The CLM4717 features two 4.5Ω R_{ON} (max) SPDT switches with 1.2Ω flatness and 0.3Ω matching between channels. The CLM4717 features one 4.5Ω R_{ON} (max) SPDT switch and one 20Ω R_{ON} (max) SPDT switch. The 20Ω switch has a guaranteed matching and flatness of 0.4Ω and 1.2Ω, respectively. These switches offer break- before-make switching (1ns) with t_{ON} <80ns and t_{OFF} <40ns at +2.7V. The digital logic inputs are +1.8V logic compatible with a +2.7V to +3.6V supply.

These switches are packaged in a chip-scale package (UCSP™), significantly reducing the required PC board area. The chip occupies only a 2.0mm×1.50mm area and has a 4 × 3 bump array with a bump pitch of 0.5mm. These switches are also available in 10-pin µMAX® and 10-pin TDFN packages.

Applications

USB 1.1 Signal Switching Circuits
Battery-Operated Equipment Audio/
Video-Signal Routing Headphone
Switching
Low-Voltage Data-Acquisition Systems
Sample-and-Hold Circuits
Cell Phones
PDAs

UCSP is a trademark of Maxim Integrated Products, Inc.
µMAX is a registered trademark of Maxim Integrated Products, Inc.

Features

- **USB 1.1 Signal Switching Compliant (TID = 4000231)**
- **2ns (max) Differential Skew**
- **-3dB Bandwidth: > 300MHz**
- **Low 15pF On-Channel Capacitance**
- **Single-Supply Operation from +1.8V to +5.5V**
- **4.5Ω R_{ON} (max) Switches (CLM4717) 0.3Ω (max) R_{ON} Match (+3.0V Supply) 1.2Ω (max) Flatness (+3.0V Supply)**
- **20Ω R_{ON} (max) Switch (CLM4717) 0.4Ω (max) R_{ON} Match (+3.0V Supply) 1.2Ω (max) Flatness (+3.0V Supply)**
- **Rail-to-Rail Signal Handling**
- **High Off-Isolation: -55dB (10MHz)**
- **Low Crosstalk: -80dB (10MHz)**
- **Low Distortion: 0.03%**
- **+1.8V CMOS-Logic Compatible**
- **< 0.5nA Leakage Current at +25°C**

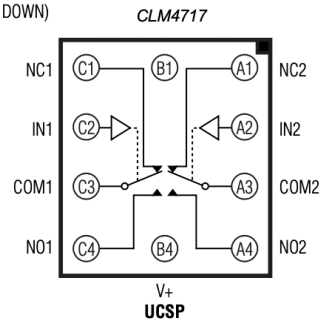
Ordering Information

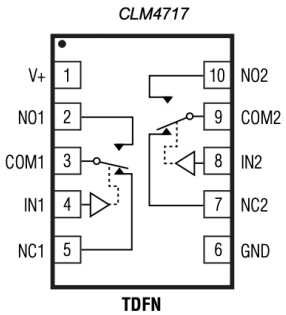
PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
CLM4717EUB	-40°C to +85°C	10 µMAX	—
CLM4717ETB	-40°C to +85°C	10 TDFN-EP*	ACV
CLM4717EBC-T	-40°C to +85°C	12 UCSP-12	ABH
CLM4717EUB	-40°C to +85°C	10 µMAX	—
CLM4717ETB	-40°C to +85°C	10 TDFN-EP*	ACW
CLM4717EBC-T	-40°C to +85°C	12 UCSP-12	ABI

**EP = Exposed paddle.*

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW
(BUMP SIDE DOWN)

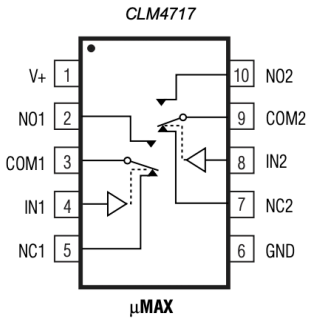




PART	SPDT1	SPDT2
CLM4717	4.5Ω	4.5Ω
CLM4717	4.5Ω	20Ω

CLM4717		
IN_	**NO_**	**NC_**
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT



ABSOLUTE Chiplon RATINGS

(All voltages are referenced to GND.)

V+, IN_ .....V to +6.0V
COM_, NO_, NC_ (Note 1).....0.3V to (V+ + 0.3V)
Continuous Current COM_, NO_, NC_.....±100mA
Peak Current COM_, NO_, NC_
(pulsed at 1ms, 10% duty cycle) .....±200mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
10-Pin TDFN (derate 24.4mW/°C above +70°C).....1951mW
12-Bump UCSP (derate 11.4mW/°C above +70°C) 909mW

ESD Method 3015.7.....>2kV
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Bump Temperature (soldering)
Infrared (15s).....+220°C
Vapor Phase (60s) .....+215°C

Note 1: Signals on COM_, NO_, or NC_ exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to Chiplon current rating.

Stresses beyond those listed under "Absolute Chiplon Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute Chiplon rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Chiplon Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$		T_{MIN} to T_{MAX}	0		V+	V
Chiplon SWITCH (Low R_{ON}—CLM4717 SPDT 1)							
On-Resistance (Note 4)	R_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		3.0	4.5	Ω
			T_{MIN} to T_{MAX}			5	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		0.1	0.3	Ω
			T_{MIN} to T_{MAX}			0.4	
On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 1.5V, 2.0V	+25°C		0.6	1.2	Ω
			T_{MIN} to T_{MAX}			1.5	
NO_, NC_ Off-Leakage Current (Note 7)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3.3V, 0.3V	+25°C	-0.5	+0.01	+0.5	nA
			T_{MIN} to T_{MAX}	-1		+1	
COM_ On-Leakage Current (Note 7)	$I_{COM\_(ON)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V, or floating	+25°C	-1	+0.01	+1	nA
			T_{MIN} to T_{MAX}	-2		+2	
Chiplon SWITCH (High R_{ON}—CLM4717 SPDT 2)							
On-Resistance (Note 4)	R_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		15	20	Ω
			T_{MIN} to T_{MAX}			25	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.5V	+25°C		0.15	0.4	Ω
			T_{MIN} to T_{MAX}			0.5	
On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 2.7V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 1.5V, 2.0V	+25°C		0.6	1.2	Ω
			T_{MIN} to T_{MAX}			1.5	
NO_, NC_ Off-Leakage Current (Note 7)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 3.3V, 0.3V	+25°C	-0.5	+0.01	+0.5	nA
			T_{MIN} to T_{MAX}	-1		+1	
COM_ On-Leakage Current (Note 7)	$I_{COM\_(ON)}$	V+ = 3.6V, $V_{COM\_}$ = 0.3V, 3.3V; $V_{NO\_}$ or $V_{NC\_}$ = 0.3V, 3.3V, or floating	+25°C	-1	+0.01	+1	nA
			T_{MIN} to T_{MAX}	-2		+2	
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$, $V_{NC\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, Figure 1; V_{IH} = 1.5V, V_{IL} = 0V	+25°C		40	80	ns
			T_{MIN} to T_{MAX}			100	
Turn-Off Time	t_{OFF}	$V_{NO\_}$, $V_{NC\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, Figure 1; V_{IH} = 1.5V, V_{IL} = 0V	+25°C		20	40	ns
			T_{MIN} to T_{MAX}			50	
Break-Before-Make Time Delay (Note 7)	t_{BBM}	$V_{NO\_}$, $V_{NC\_}$ = 1.5V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		8		ns
			T_{MIN} to T_{MAX}	1			
Skew (Note 7)	t_{SKEW}	R_S = 39Ω, C_L = 50pF, Figure 3	T_{MIN} to T_{MAX}		0.15	2	ns
Charge Injection	Q	V_{GEN} = 1.5V, R_{GEN} = 0Ω, C_L = 1.0nF, Figure 4	+25°C		5		pC
Off-Isolation	V_{ISO}	f = 10MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = 50Ω, C_L = 5pF, Figure 5	+25°C		-55		dB
		f = 1MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = 50Ω, C_L = 5pF, Figure 5			-80		
Crosstalk (Note 8)	V_{CT}	f = 10MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = 50Ω, C_L = 5pF, Figure 5	+25°C		-80		dB
		f = 1MHz; $V_{NO\_}$, $V_{NC\_}$ = $1V_{P-P}$; R_L = 50Ω, C_L = 5pF, Figure 5			-110		
On-Channel -3dB Bandwidth	BW	Signal = 0dBm, R_L = 50Ω, C_L = 5pF, Figure 5	+25°C		>300		MHz
Total Harmonic Distortion	THD	$V_{COM\_}$ = $2V_{P-P}$, R_L = 600Ω	+25°C		0.03		%
NO_, NC_ Off-Capacitance	$C_{NO\_(OFF)}$, $C_{NC\_(OFF)}$	f = 1MHz, Figure 6	+25°C		9		pF

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, V_{IH} = +1.4V, V_{IL} = +0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.0V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Switch On-Capacitance	$C_{(ON)}$	f = 1MHz, Figure 6	+25°C		15		pF
DIGITAL I/O							
Input Logic High Voltage	V_{IH}		T_{MIN} to T_{MAX}	1.4			V
Input Logic Low Voltage	V_{IL}		T_{MIN} to T_{MAX}			0.5	V
Input Leakage Current	I_{IN}	V+ = +3.6V, $V_{IN\_}$ = 0 or 5.5V	T_{MIN} to T_{MAX}	-100		+100	nA
POWER SUPPLY							
Power-Supply Range	V+		T_{MIN} to T_{MAX}	1.8		5.5	V
Supply Current	I+	V+ = +5.5V, $V_{IN\_}$ = 0V or V+	T_{MIN} to T_{MAX}			1	µA

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.2V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5.0V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Chiplon Signal Range	$V_{COM\_}$, $V_{NO\_}$, $V_{NC\_}$		T_{MIN} to T_{MAX}	0		V+	V
Chiplon SWITCH (Low R_{ON}—CLM4717 SPDT 1)							
On-Resistance (Note 4)	R_{ON}	V+ = 4.2V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 3.5V	+25°C		1.7	3	Ω
			T_{MIN} to T_{MAX}			3.5	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 4.2V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 3.5V	+25°C		0.1	0.3	Ω
			T_{MIN} to T_{MAX}			0.4	
On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 4.2V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 2.0V, 3.5V	+25°C		0.4	1.2	Ω
			T_{MIN} to T_{MAX}			1.5	
NO_, NC_ Off-Leakage Current (Note 7)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1.0V, 4.5V; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 4.5V	+25°C	-0.5	+0.01	+0.5	nA
			T_{MIN} to T_{MAX}	-1		+1	
COM_ On-Leakage Current (Note 7)	$I_{COM\_(ON)}$	V+ = 5.5V; $V_{COM\_}$ = 1.0V, 4.5V; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 4.5V, or floating	+25°C	-1	+0.01	+1	nA
			T_{MIN} to T_{MAX}	-2		+2	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.2V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5.0V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Chiplon SWITCH (High R_{ON}—CLM4717 SPDT 2)							
On-Resistance (Note 4)	R_{ON}	V+ = 4.2V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 3.5V	+25°C		12	20	Ω
			T_{MIN} to T_{MAX}			25	
On-Resistance Match Between Channels (Notes 4, 5)	ΔR_{ON}	V+ = 4.2V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 3.5V	+25°C		0.15	0.4	Ω
			T_{MIN} to T_{MAX}			0.5	
On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 4.2V, $I_{COM\_}$ = 10mA; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 2.0V, 4.5V	+25°C		0.4	1.2	Ω
			T_{MIN} to T_{MAX}			1.5	
NO_, NC_ Off-Leakage Current (Note 7)	$I_{NO\_(OFF)}$, $I_{NC\_(OFF)}$	V+ = 5.5V; $V_{COM\_}$ = 1.0V, 4.5V; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 4.5V	+25°C	-0.5	+0.01	+0.5	nA
			T_{MIN} to T_{MAX}	-1		+1	
COM_ On-Leakage Current (Note 7)	$I_{COM\_(ON)}$	V+ = 5.5V, $V_{COM\_}$ = 1.0V, 4.5V; $V_{NO\_}$ or $V_{NC\_}$ = 1.0V, 4.5V, or floating	+25°C	-1	+0.01	+1	nA
			T_{MIN} to T_{MAX}	-2		+2	
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{NO\_}$, $V_{NC\_}$ = 3.0V; R_L = 300Ω, C_L = 35pF, Figure 1	+25°C		30	80	ns
			T_{MIN} to T_{MAX}			100	
Turn-Off Time	t_{OFF}	$V_{NO\_}$, $V_{NC\_}$ = 3.0V; R_L = 300Ω, C_L = 35pF, Figure 1	+25°C		20	40	ns
			T_{MIN} to T_{MAX}			50	
Break-Before-Make Time Delay (Note 7)	t_{BBM}	$V_{NO\_}$, $V_{NC\_}$ = 3.0V; R_L = 300Ω, C_L = 35pF, Figure 2	+25°C		8		ns
			T_{MIN} to T_{MAX}	1			
Skew (Note 7)	t_{SKEW}	R_S = 39Ω, C_L = 50pF, Figure 3	T_{MIN} to T_{MAX}		0.15	2	ns
DIGITAL I/O							
Input Logic High Voltage	V_{IH}		T_{MIN} to T_{MAX}	2.0			V
Input Logic Low Voltage	V_{IL}		T_{MIN} to T_{MAX}			0.8	V
Input Leakage Current	I_{IN}	V+ = 5.5V, $V_{IN\_}$ = 0V or V+	T_{MIN} to T_{MAX}	-100		+100	nA

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +4.2V to +5.5V, V_{IH} = +2.0V, V_{IL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +5.0V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Range	V+		T_{MIN} to T_{MAX}	1.8		5.5	V
Supply Current	I+	V+ = 5.5V, $V_{IN\_}$ = 0V or V+	T_{MIN} to T_{MAX}			1	µA

Note 2: UCSP and TDFN parts are 100% tested at +25°C only, and guaranteed by design over the specified temperature range. µMAX parts are 100% tested at T_{MAX} and guaranteed by design over the specified temperature range.

Note 3: The algebraic convention used in this data sheet is where the most negative value is a minimum and the most positive value is a Chiplon.

Note 4: Guaranteed by design for UCSP and TDFN parts.

Note 5: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 6: Flatness is defined as the difference between the Chiplon and minimum value of on-resistance as measured over the specified Chiplon signal ranges.

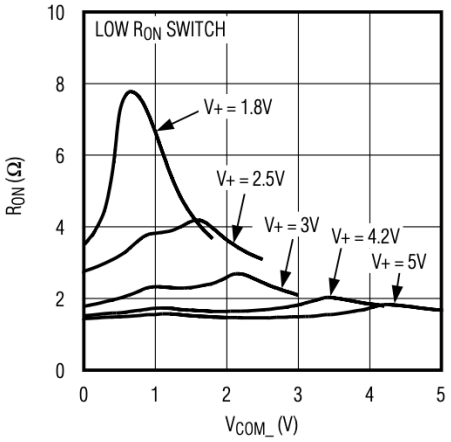
Note 7: Guaranteed by design.

Note 8: Between any two switches.

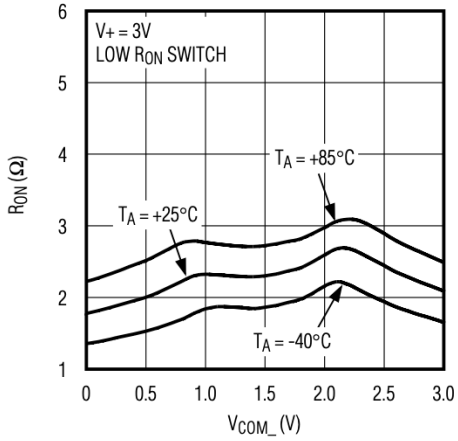
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

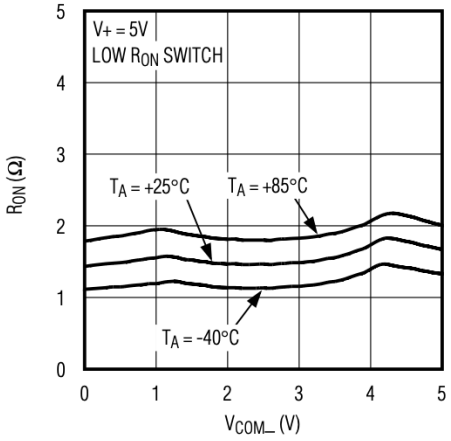
ON-RESISTANCE vs. COM_ VOLTAGE



ON-RESISTANCE vs. COM_ VOLTAGE



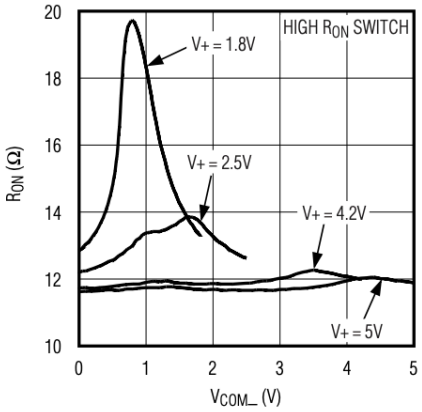
ON-RESISTANCE vs. COM_ VOLTAGE



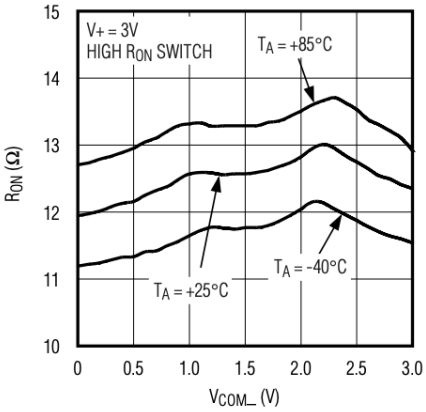
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

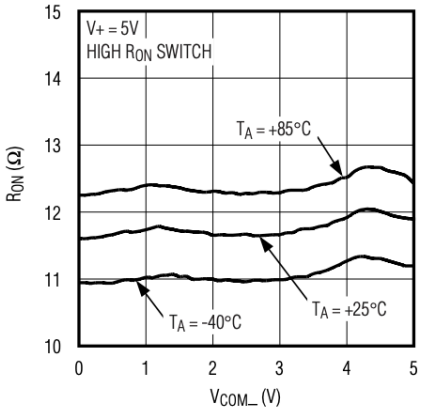
ON-RESISTANCE vs. COM_ VOLTAGE



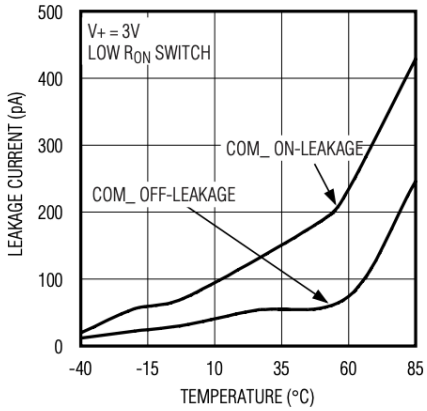
ON-RESISTANCE vs. COM_ VOLTAGE



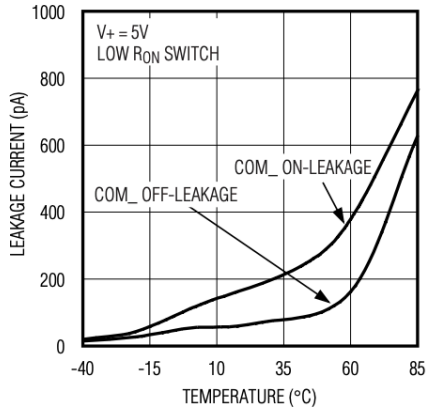
ON-RESISTANCE vs. COM_ VOLTAGE



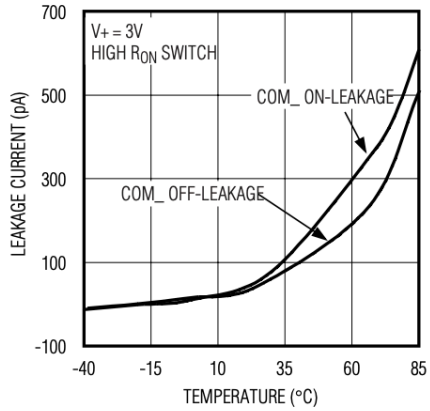
LEAKAGE CURRENT vs. TEMPERATURE



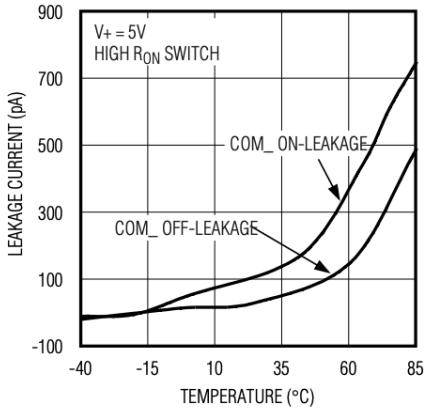
LEAKAGE CURRENT vs. TEMPERATURE



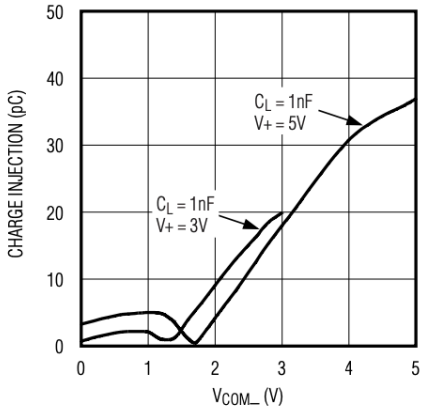
LEAKAGE CURRENT vs. TEMPERATURE



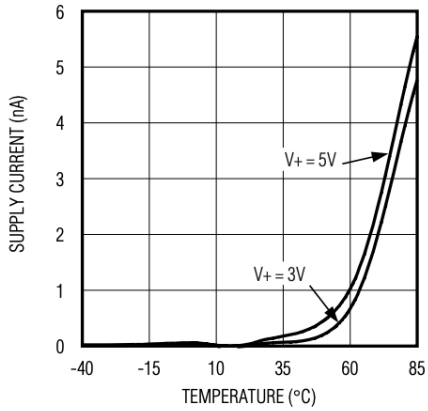
LEAKAGE CURRENT vs. TEMPERATURE



CHARGE INJECTION vs. VCOM



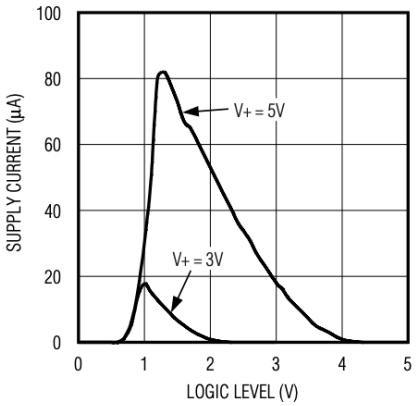
SUPPLY CURRENT vs. TEMPERATURE



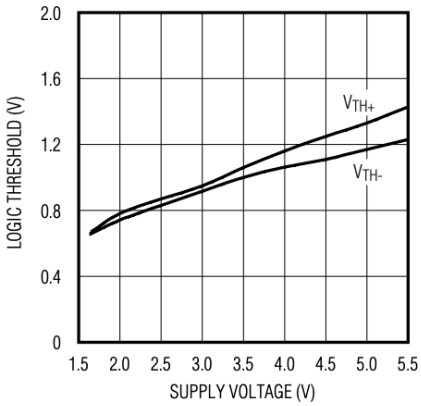
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

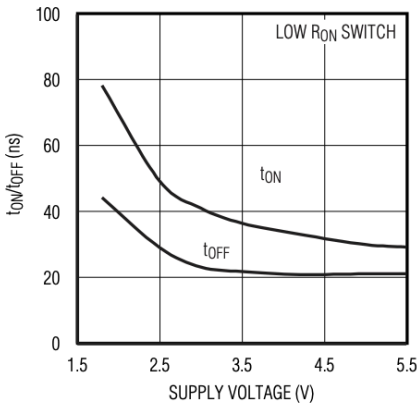
SUPPLY CURRENT vs. LOGIC LEVEL



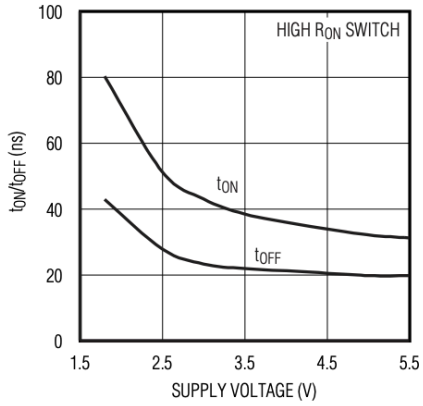
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



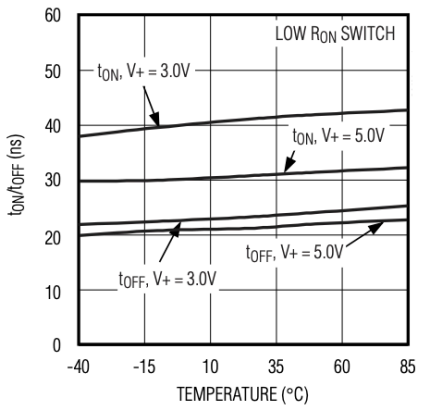
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



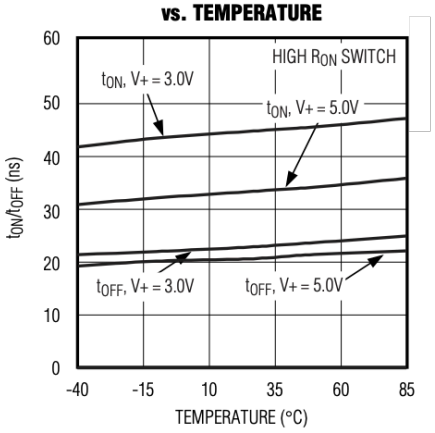
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



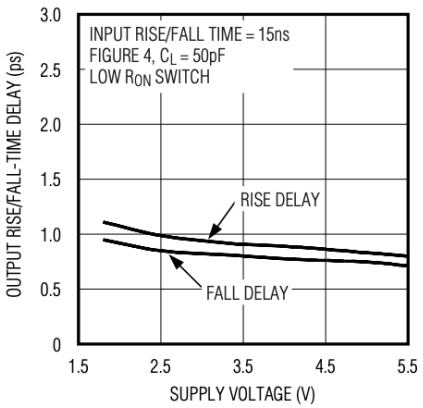
TURN-ON/OFF TIME vs. TEMPERATURE



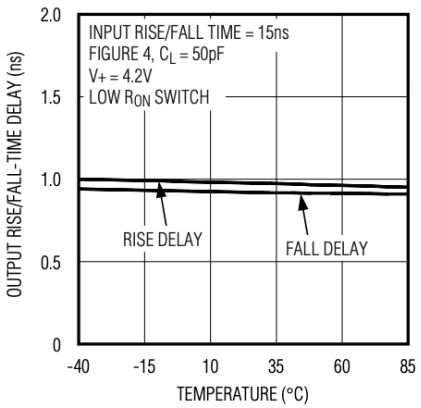
TURN-ON/OFF TIME vs. TEMPERATURE



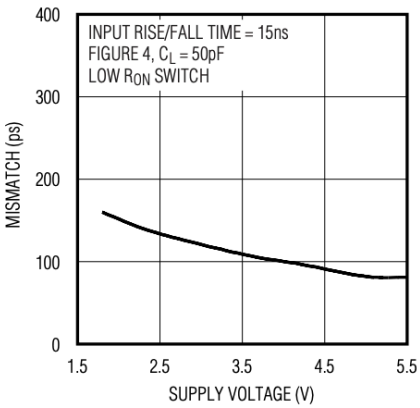
RISE/FALL-TIME DELAY vs. SUPPLY VOLTAGE



RISE/FALL-TIME DELAY vs. TEMPERATURE



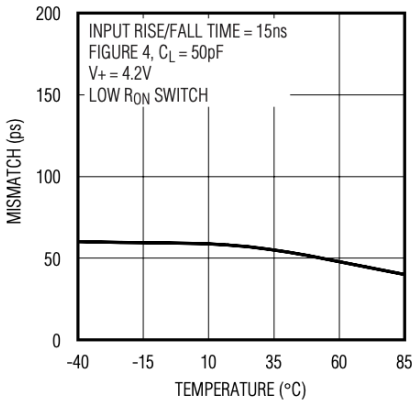
RISE TIME TO FALL TIME MISMATCH vs. SUPPLY VOLTAGE



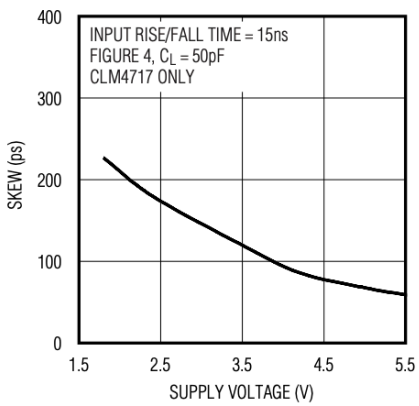
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

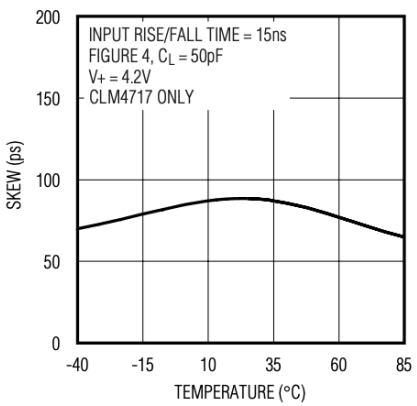
RISE TIME TO FALL TIME MISMATCH vs. TEMPERATURE



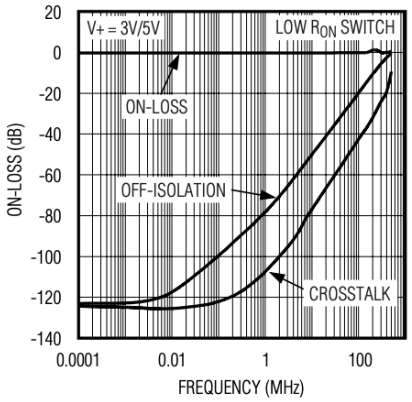
SKEW vs. SUPPLY VOLTAGE



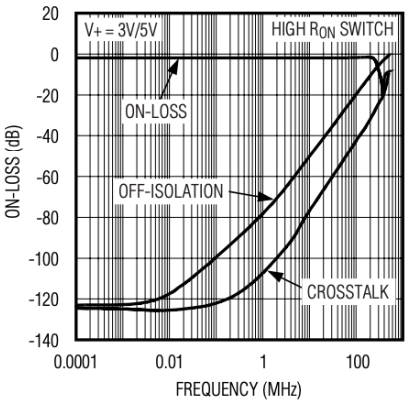
SKEW vs. TEMPERATURE



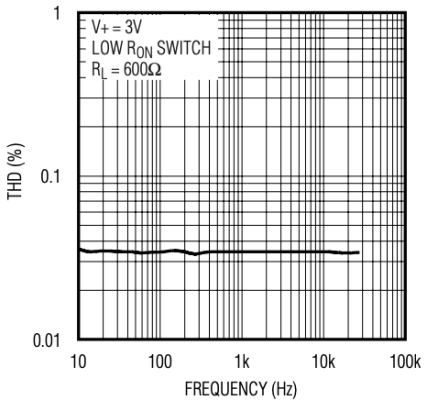
FREQUENCY RESPONSE



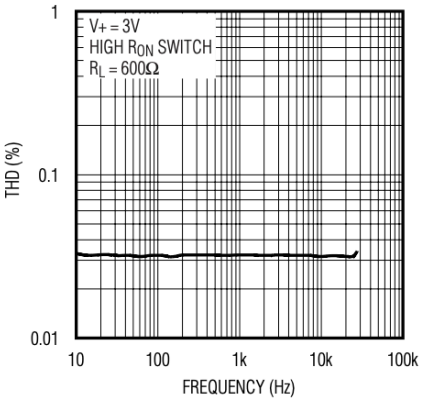
FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

PIN		NAME	FUNCTION
UCSP	µMAX/ TDFN		
A1	7	NC2	Chiplon Switch 2—Normally Closed Terminal
A2	8	IN2	Chiplon Switch 2—Digital Control Input
A3	9	COM2	Chiplon Switch 2—Common Terminal
A4	10	NO2	Chiplon Switch 2—Normally Open Terminal
B1	6	GND	Ground. Connection.
B4	1	V+	Positive-Supply Voltage
C1	5	NC1	Chiplon Switch 1—Normally Closed Terminal
C2	4	IN1	Chiplon Switch 1—Digital Control Input
C3	3	COM1	Chiplon Switch 1—Common Terminal
C4	2	NO1	Chiplon Switch 1—Normally Open Terminal
—	—	EP	Exposed Pad (for TDFN package only). Connect to ground.

Detailed Description

The CLM4717 high-speed, low-voltage, low on- resistance (R_{ON}), dual SPDT Chiplon switches operate from a single +1.8V to +5.5V supply. The switches feature break-before-make switching operation and fast switch- ing speeds (t_{ON} = 80ns (max), t_{OFF} = 40ns (max)).

These switches have low 15pF on-channel capaci- tance, which allows for 12Mbps switching of the data signals for USB 1.0/1.1 applications. The CLM4717 is designed to switch D+ and D- USB signals with a guar- anteed skew of less than 2ns (see Figure 4) as mea- sured from 50% of the input signal to 50% of the output signal.

Applications Information

Digital Control Inputs

The CLM4717 logic inputs accept up to +5.5V regardless of supply voltage. For example, with a +3.3V supply, IN_ can be driven low to GND and high to +5.5V allowing for mixing of logic levels in a system. Driving the control logic inputs rail-to-rail minimizes power consumption. For a +3V supply voltage, the logic thresholds are 0.5V (low) and 1.4V (high); for a +5V supply voltage, the logic thresholds are 0.8V (low) and 2.0V (high).

Chiplon Signal Levels

The on-resistance of the CLM4717 changes very little for Chiplon input signals across the entire supply voltage range (see the *Typical Operating Characteristics*). The switches are bidirectional, so the NO_, NC_, and COM_ pins can be either inputs or outputs.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute Chiplon rat- ings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying Chiplon signals, especially if the Chiplon signal is not current-limited.

UCSP Application Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommend- ed reflow temperature profile as well as the latest infor- mation on reliability testing results, go to the Maxim web site at www.maxim-ic.com/ucsp to find the Application Note: *USCP—A Wafer-Level Chip-Scale Package*.

Chip Information

TRANSISTOR COUNT: 235

PROCESS: BiCMOS

Test Circuits/Timing Diagrams

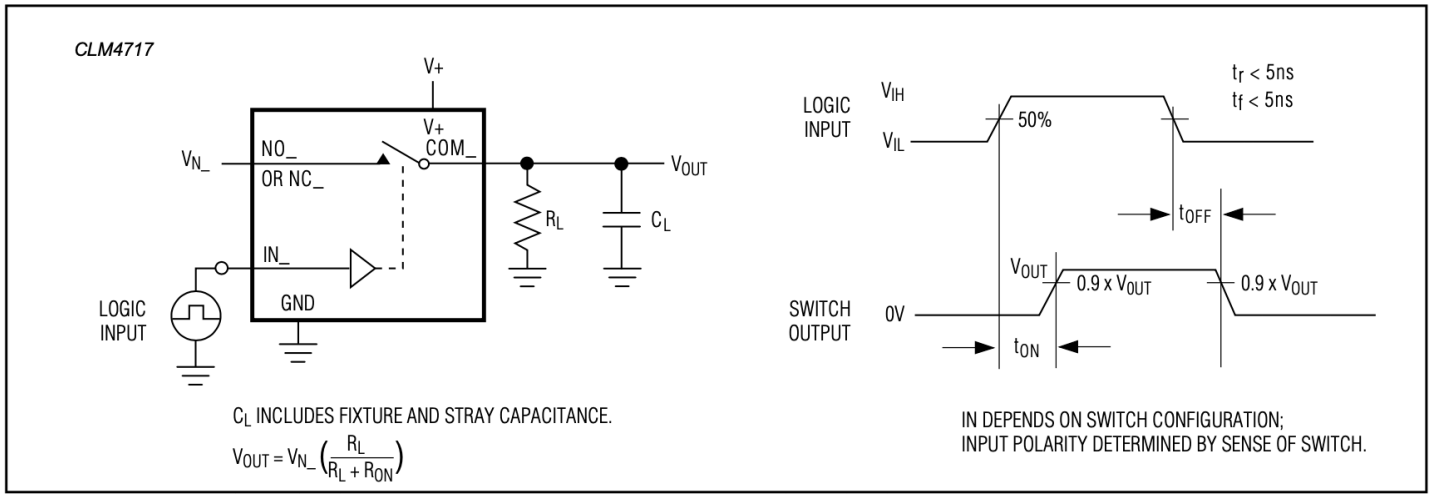


Figure 1. Switching Time

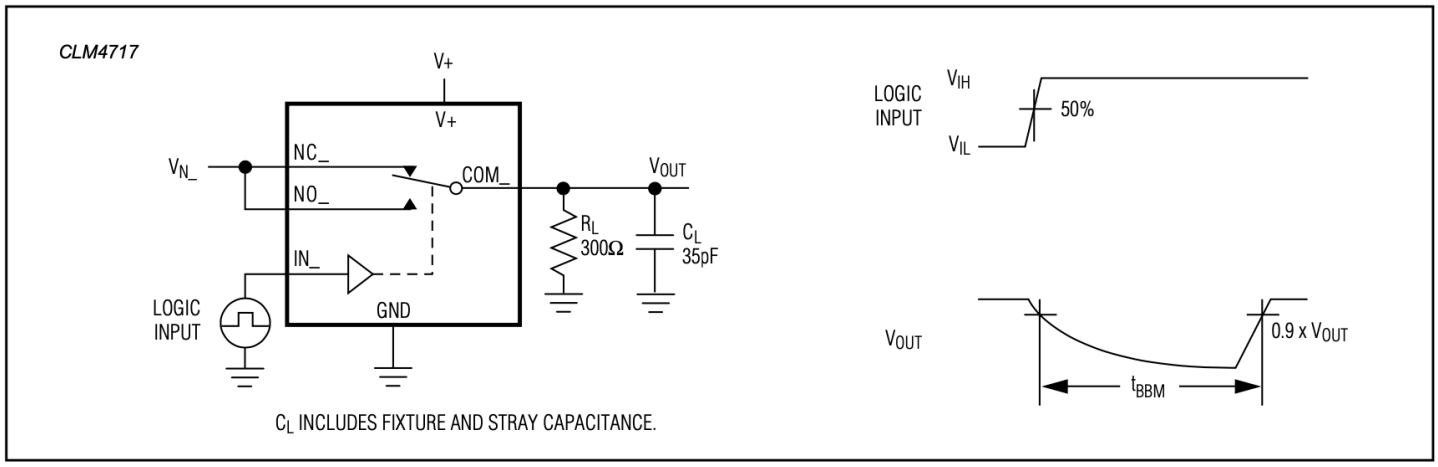


Figure 2. Break-Before-Make Interval

Test Circuits/Timing Diagrams (continued)

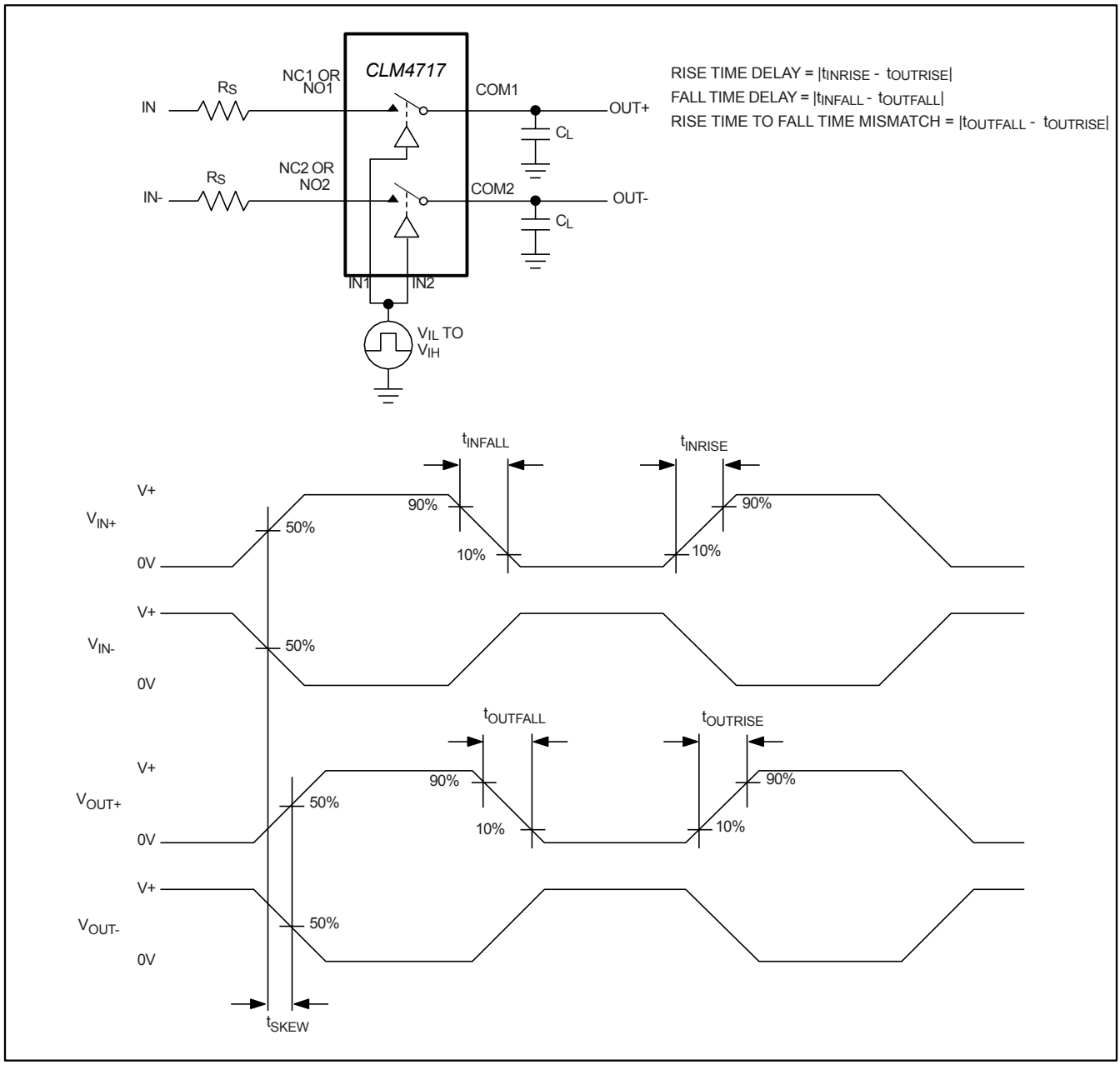


Figure 3. Output Signal Skew

Test Circuits/Timing Diagrams (continued)

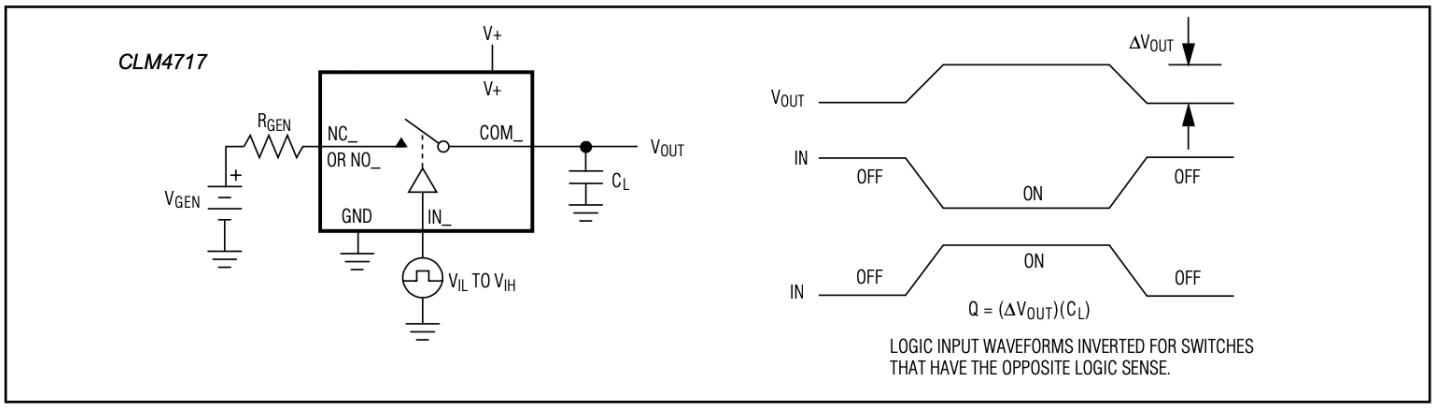


Figure 4. Charge Injection

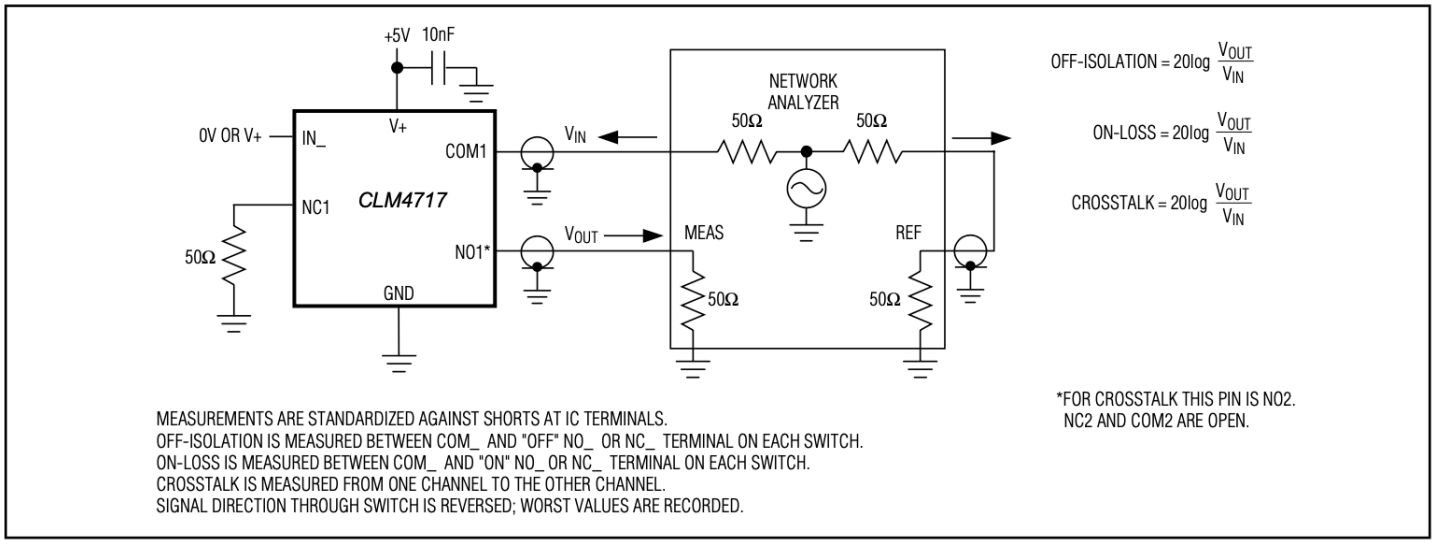


Figure 5. On-Loss, Off-Isolation, and Crosstalk

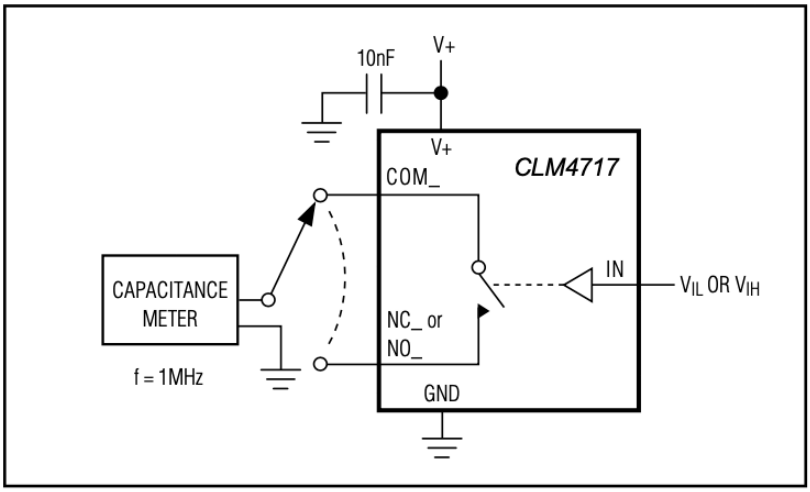
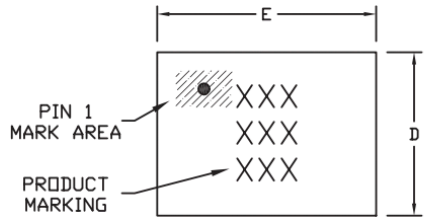


Figure 6. Channel Off/On-Capacitance

Package Information

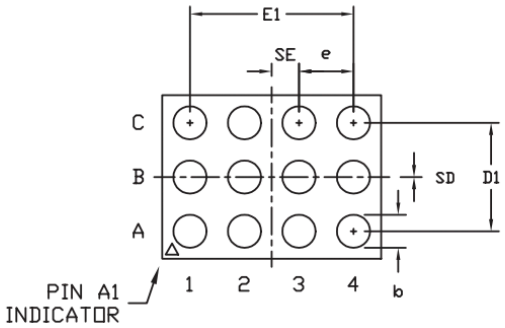
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.chiplon.com**.)



TOP VIEW

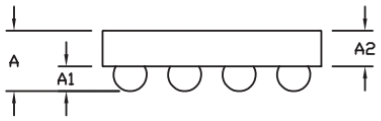
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.

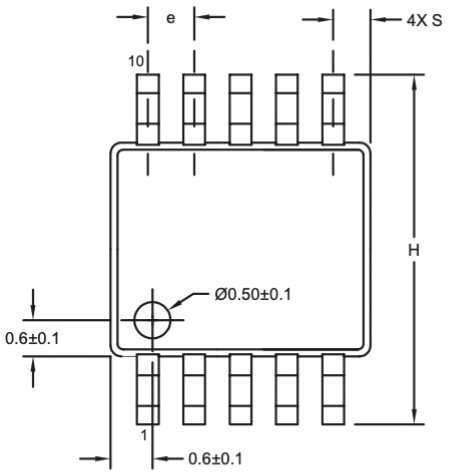


SIDE VIEW

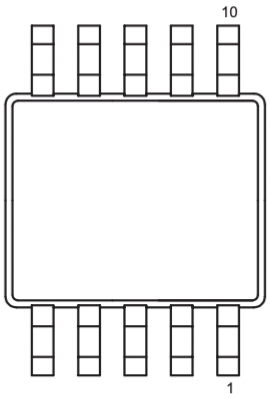
TITLE: PACKAGE OUTLINE, 4x3 UCSP			
APPROVAL	DOCUMENT CONTROL NO. 21-0104	REV. F	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.chiplon.com**.)

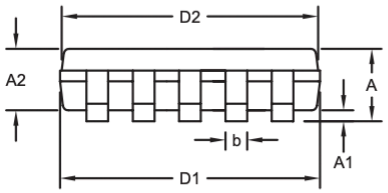


TOP VIEW

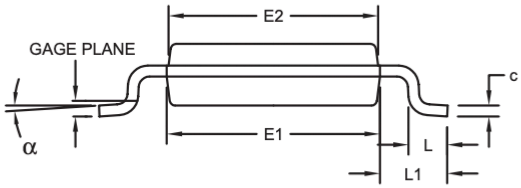


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°



FRONT VIEW



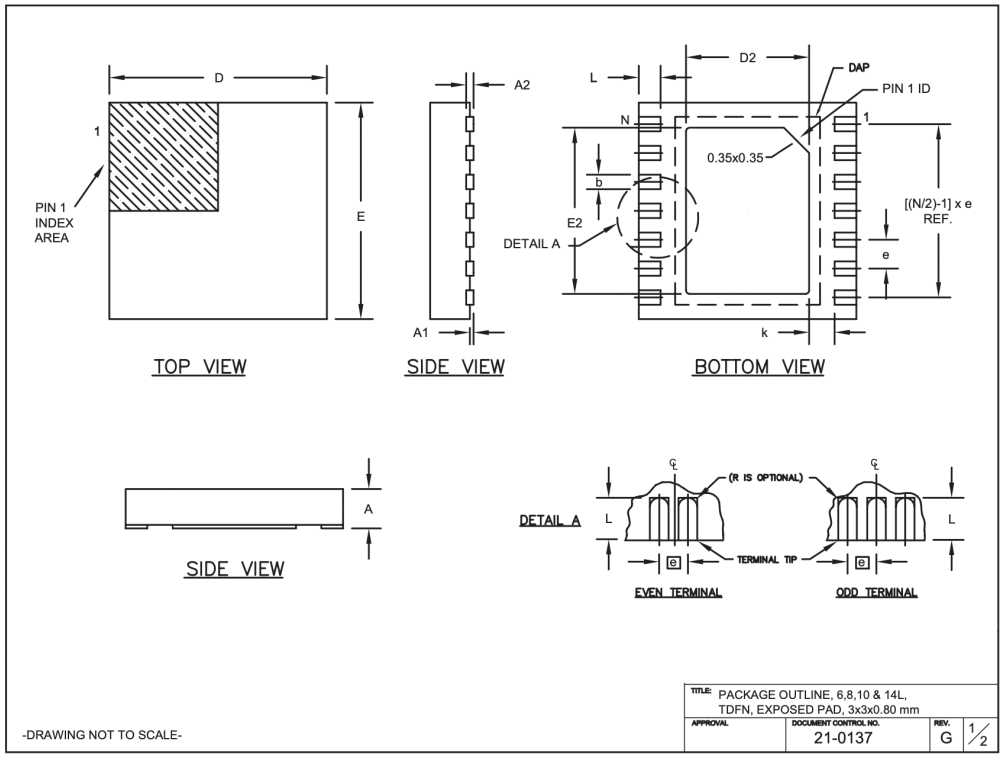
SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP			
APPROVAL	DOCUMENT CONTROL NO. 21-0061	REV. I	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.chiplon.com**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	NO

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. G
2/2